APPLICATION OF THREE-PHASE FOUR-WIRE ACTIVE FILTER FOR SHUNT AND SERIES COMPENSATION IN SYSTEMS WITH NON-IDEAL SUPPLY

A thesis submitted in partial fulfillment of the requirements for the Degree of

Master of Technology

by

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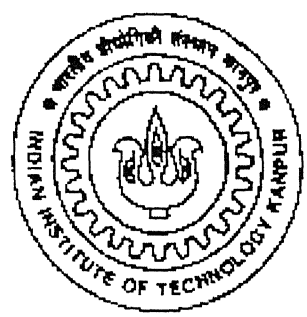

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CERTIFICATE

This is to certify that the work contained in the thesis entitled **"Application of Three-phase Four-wire Active Filter for Shunt and Series Compensation in Systems with Non-ideal Supply"** by **Shivkumar Venkatraman Iyer** has been carried out under our supervision and this work has not been submitted elsewhere for a degree.

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Dedicated to my parents and

my elder sister

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Shivkumar .V. Iyer

ABSTRACT

The dramatic rise of power electronic converters, rectifiers and cycloconverters besides an increased incidence of unbalanced loads has resulted in distortion and unbalance in the currents drawn from the supply and in the voltages at the Point of Common Coupling (PCC). The high harmonic content of the current in the system could cause overheating in transformers and other electric machines. Unbalance in loads as well as widespread use of single-phase converters will result in high current in the neutral. As the distortions in the PCC voltage would affect all the loads connected at the PCC, there arises a need to filter out the harmonics drawn by the non-linear load and further provide some power factor correction at the PCC. For improved harmonic filtering, power factor correction and voltage regulation active filters are replacing the older passive filters. Shunt active filters have been studied and simulated in this thesis for the purpose of harmonic filtering, power factor correction and voltage regulation at the PCC. Existing algorithms used for generating references for injected currents have been reviewed and a new algorithm has been proposed to overcome their drawbacks. Inverter topologies used to realize the shunt active filters have been compared as well as filter structures for bypassing high frequency components and control strategies have been discussed and implemented. Simulation studies have considered all possible disturbances in the supply and the source and the performance of the shunt active filter have been studied. For the purpose of load voltage regulation series active filters have also been discussed. As with shunt active filters, a comparison of inverter topologies and filter structures has been done for the series active filter as well. To regulate the load voltage against deep sags in the source voltage auxiliary supply of power to the DC link through a rectifier has been simulated and the results will show that the load voltage has been completely regulated despite the poor quality of the source voltages.

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LIST OF SYMBOLS

v_{sa}, v_{sb}, v_{sc}	Source voltages of phase *a*, *b* and *c* respectively
i_{sa}, i_{sb}, i_{sc}	Source currents in phases *a*, *b* and *c* respectively
i_{la}, i_{lb}, i_{lc}	Load currents in phases *a*, *b* and *c* respectively
v_{ta}, v_{tb}, v_{tc}	Terminal voltages of phase *a*, *b* and *c* respectively
$i^*_{fa}, i^*_{fb}, i^*_{fc}$	References for currents injected into the system in phase *a*, *b* and *c* respectively
i_{fa}, i_{fb}, i_{fc}	Actual currents injected into the system in phase *a*, *b* and *c* respectively
$i^*_{da}, i^*_{db}, i^*_{dc}$	References for currents injected by the inverter in phase *a*, *b* and *c* respectively
i_{da}, i_{db}, i_{dc}	Actual currents injected by the inverter in phase *a*, *b* and *c* respectively
$i^*_{cfa}, i^*_{cfb}, i^*_{cfc}$	References for currents through the filter capacitors in phase *a*, *b* and *c* respectively
$i_{cfa}, i_{cfb}, i_{cfc}$	Actual currents through the filter capacitors in phase *a*, *b* and *c* respectively
p_l, p_s	Total three-phase instantaneous real power of the load and source respectively
$\overline{p}_l, \overline{p}_s$	Average component of the total instantaneous real power of the load and source respectively
$\widetilde{p}_l, \widetilde{p}_s$	Zero mean oscillating component of the total instantaneous real power of the load and source respectively
q_{la}, q_{lb}, q_{lc}	Instantaneous reactive power absorbed by the load in phase *a*, *b* and *c* respectively
q_{sa}, q_{sb}, q_{sc}	Instantaneous reactive power supplied by the source in phase *a*, *b* and *c* respectively
q_l, q_s	Total three-phase instantaneous reactive power of the load and source respectively
$\overline{q}_l, \overline{q}_s$	Average component of the total instantaneous reactive power of the load and source respectively
$\widetilde{q}_l, \widetilde{q}_s$	Zero mean oscillating component of the total instantaneous

	reactive power of the load and source respectively
p_{loss}	Losses in the inverter
$V_{taf}, V_{tbf}, V_{tcf}$	Fundamental terminal voltage phasors of phase *a*, *b* and *c* respectively
$V_{taf0}, V_{taf1}, V_{taf2}$	Fundamental zero, positive and negative sequence terminal voltage phasors
$I_{sa0}, I_{sa1}, I_{sa2}$	Fundamental zero, positive and negative sequence phasors for source currents
ϕ	Phase angle between the terminal voltages and source currents of the respective phases
I_{sa}, I_{sb}, I_{sc}	Source current phasors of phase *a*, *b* and *c* respectively
v_{cref}, v_c	Reference and actual value of the voltage across dc capacitor
K_p, K_I	Proportional and integral time constant of the PI controller
$\phi^*_{ta}, \phi^*_{tb}, \phi^*_{tc}$	Reference phase angles of the terminal voltages of phase *a*, *b* and *c* respectively
$v^*_{ta}, v^*_{tb}, v^*_{tc}$	Reference terminal voltages of phase *a*, *b* and *c* respectively
$v^*_{da}, v^*_{db}, v^*_{dc}$	References for the series injected voltages of phase *a*, *b* and *c* respectively
R_s, L_s	Resistance and inductance of the feeder
L_{da}, L_{db}, L_{dc}	Filter inductances connected to the *a*, *b* and *c* phases of the inverter
C_{fa}, C_{fb}, C_{fc}	Filter capacitances connected to the *a*, *b* and *c* phases of the PCC in series compensation
L_{fa}, L_{fb}, L_{fc}	Filter inductances connected in the *a*, *b* and *c* phases just before the PCC in series compensation
C_{da}, C_{db}, C_{dc}	Filter capacitances connected across the isolation transformers in phases *a*, *b* and *c* in series compensation
L_T, R_T	Leakage reactance and winding resistance of the isolation transformers
u_c	Continuous control input signal obtained from the controller
u	Switching control logic for the inverter
$\boldsymbol{Q}, r$	State weighting matrix and control weighting used for LQR state feedback controller

K', K	Complete and reduced feedback matrix obtained for LQR state feedback controller

CHAPTER 1

INTRODUCTION

The past few decades have witnessed a dramatic rise in the use of power electronic devices due to their high efficiency. The use of power electronic converters, inverters and cycloconverters causes harmonic pollution in the distribution system. Besides power electronic devices, loads in a distribution system can be unbalanced. The adverse effects of power electronic devices and unbalanced loads can be summarized as follows

- Unbalanced and distorted currents drawn from the utility.
- Unbalanced and distorted voltages.
- Excessive neutral current in three-phase four-wire systems.
- High neutral-to-ground voltage in a three-phase three-wire system.
- Overheating in electric machines and transformers.

Due to the above effects, the need arises to provide balanced and sinusoidal voltages especially to certain sensitive loads. Most often it is the sensitive loads that are responsible for polluting the distribution system. Earlier methods of load compensation have been based on passive filters such as tuned LC filters. The drawbacks of the passive filters are

- A separate filter is required to filter a particular harmonic component in the load current.
- The filter may absorb power at the fundamental frequency.
- The filter may cause resonance in the circuit.
- The filter is unable to provide power factor correction.

Active filters have gained importance in recent times. Active filters are inverter-based filters having power electronic switches such as Insulated Gate Bipolar Transistors (IGBTs) or Gate Turn-off Thyristors (GTOs). PWM control strategies and improved control algorithms implemented using DSP processors and single-board computers has made active filters an attractive solution. The advantages of active filters over passive filters can be summarized as follows

- A single active filter is capable of removing almost all the harmonic components in the load current.
- The active filter can be made to neither absorb nor supply any real power at the fundamental frequency.
- The active filter can provide damping in the circuit.
- The active filter is capable of correcting power factor.

A few disadvantages of active filters may be listed as follows

- An active filter will require a reference for the current to be injected in shunt or the voltage to be injected in series. To generate references a digital computer or a DSP processor will be required.
- The active filter will be having power electronic switches as mentioned before. These switches will have to be turned on and off using control signals that are complex to generate.

1.1 CLASSIFICATION OF ACTIVE FILTERS

Active filters can be classified as Voltage Source Inverters (VSI) or Current Source Inverters (CSI). In VSIs, the energy storage element is either a DC battery or a large DC storage capacitor. Fig. 1.1 shows the circuit diagram of a three-leg VSI. The switches shown are IGBTs or GTOs with their associated anti-parallel diodes. They have the advantage of good response times and can be easily expanded to multilevel inverters. However, there is a greater chance of short circuit of the energy storage element in the event of both switches in a leg being closed at the same time. Due to the application of better control strategies the risk has been reduced considerably.

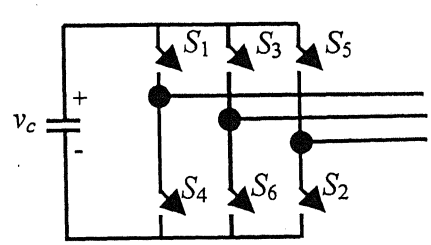

Fig. 1.1 Three-leg VSI

In CSIs, the energy storage element is a large inductor. The inductor could be made of a super conducting material to minimize the losses. Fig. 1.2 shows the circuit

diagram of a three-leg CSI. The response of this inverter is slower than the VSI and is not easily expandable to multilevel inverters. However the risk of damage of the switches due to the short circuit of the energy storage element is lesser because the current through the inductor cannot rise instantaneously.

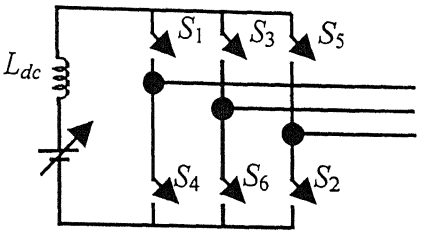

Fig. 1.2 Three-leg CSI

Active filters can be further classified based on the method of connection – shunt or series. A shunt active filter is called a Distribution Static Compensator (DSTATCOM) while a series active filter is called a Dynamic Voltage Regulator (DVR). The next two sections will describe the DSTATCOM and the DVR.

1.2 DISTRIBUTION STATIC COMPENSATOR (DSTATCOM)

The single line diagram of the DSTATCOM is shown in Fig. 1.3. The DSTATCOM is a current injection device which injects currents into the Point of Common Coupling (PCC). However, the DSTATCOM can be made to operate in the current control mode or the voltage control mode.

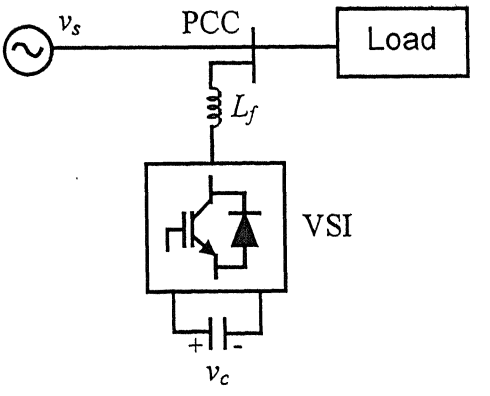

Fig. 1.3 DSTATCOM using a VSI

1.2.1 DSTATCOM in Current Control Mode

In the current control mode, the DSTATCOM injects currents into the PCC so as to make the source currents balanced, sinusoidal and at a desired phase angle with

respect to the PCC voltages. Different inverter topologies have been used to compensate for harmonics and reactive power of the load, some of which are the three-leg inverter with single DC capacitor, three-leg inverter with neutral clamped DC capacitors, four-leg inverter and three independent inverters with single DC capacitor. Several methods for generating references for compensator currents have been proposed and implemented [4-8]. Different types of current controllers have been studied for tracking the references for the compensator current [11]. In addition to the conventional hysteresis control and PWM control, more complex control algorithms such as the Linear Quadratic Regulator (LQR), pole shift controller and deadbeat controller have been implemented.

1.2.2 DSTATCOM in Voltage Control Mode

In the voltage control mode, the DSTATCOM injects currents into the PCC so that the PCC voltages are balanced sinusoids and regulated to a fixed peak. The deadbeat controller has been used to control a three-leg inverter with neutral clamped DC capacitors for the above purpose [17]. Other forms of control such as LQR control have also been studied [9].

1.3 DYNAMIC VOLTAGE REGULATOR (DVR)

The DVR is a series compensation device which regulates the voltage at the load bus against distortions in the source voltages. Fig. 1.4 shows the single-line diagram of a DVR.

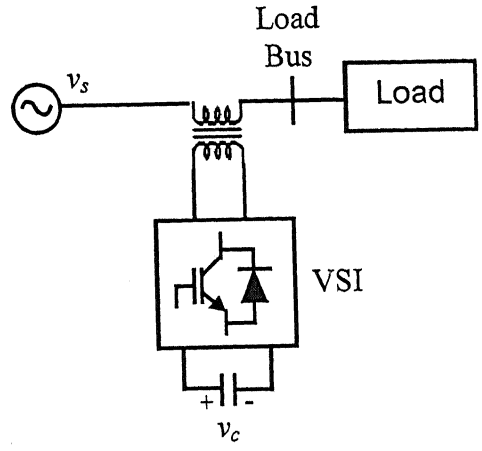

Fig. 1.4 DVR using a VSI

As with the DSTATCOM, various inverter topologies have been used such as the three-leg inverter with single DC capacitor and three independent inverters with single DC capacitor. Besides the conventional PWM control strategy, more complex control strategies such as deadbeat control, pole shift control and state feedback control have been used for controlling the switching of the inverter. The DVR has also been made to restore the voltage to a fixed peak when the source voltages dip [22-24].

1.4 OBJECTIVE OF THE THESIS

The objectives of the thesis can be summarized as follows

1. To compare the performance of different topologies of VSIs for the DSTATCOM and their applications to different types of distribution systems.
2. To develop an algorithm for generating references for currents to be injected by the DSTATCOM in current control mode when the source is non-stiff, unbalanced and distorted and to ensure that the active filter neither absorbs nor supplies any real power in the steady state.
3. To compare different control strategies for DSTATCOM in current control mode through simulation studies.
4. To simulate the DSTATCOM in the voltage control mode for all possible disturbances in the source and load.
5. To compare the performance of different topologies of VSIs for the DVR and their applications to different system conditions.
6. To simulate a DVR which is capable of regulating the load voltages for all disturbances in the source.

With reference to the research already published, the contributions of the thesis are as follows

1. Different inverter topologies have been used for shunt and series active filters in the entire list of references provided. A comparison of the different inverter topologies has been performed using simulations and graphs have been presented to select the three-phase four-leg VSI with single DC capacitor as the best topology. All simulations have been performed using PSCAD/EMTDC (Version 3.0.7). However, the simulation data have been transferred to MATLAB for plotting.

2. Several algorithms have been presented for generating references for currents to be injected by the DSTATCOM so as to make the source currents balanced sinusoids. Most of the algorithms are based on the instantaneous reactive power theory and are capable of compensating systems with balanced source voltages [7, 8]. However, these algorithms fail when applied to systems with source voltages that are not balanced sinusoids. Algorithms have been proposed to compensate such systems with non-ideal voltages [4, 5, 6]. The algorithm in [4] is applicable only to three-phase three-wire systems. The algorithm in [5] does not force the condition that the DSTATCOM should not absorb or supply any real power in the steady state. The algorithm in [6] has been formulated for a system with a stiff source and hence will have to be modified for a non-stiff source. To overcome the shortcomings of the algorithms mentioned above, a new algorithm has been developed based on phasor quantities rather than instantaneous quantities. The algorithm has been proved to be effective by performing a simulation considering a system with a non-stiff, unbalanced and distorted source.
3. A comparison of controllers such as the hysteresis controller, ramp controller etc for the DSTATCOM has been performed in [11]. More complex controllers such as the deadbeat controller, pole shift controller and LQR controller have been discussed and used for controlling active filters in [9]. A comparison between controllers has been performed in this thesis supported by simulation results. The LQR controller has been found to be most suitable when the system voltages are balanced sinusoids while the pole shift controller has been selected as the best controller when the system voltages maybe unbalanced or distorted or both.
4. Different inverter topologies for the DVR have been compared and simulation results have been presented. The four-leg VSI with single DC capacitor has been selected as the best. The DVR with the above topology has been supported by a rectifier to compensate for unbalance, distortions and dip in the source voltages and has been shown to provide complete compensation for all disturbances from the source.

1.5 OUTLINE OF THE THESIS

Chapter 2 compares the VSI topologies for the DSTATCOM and the DVR providing simulation results for each topology.

Chapter 3 describes the DSTATCOM in current control mode. A new algorithm has been developed for compensating systems with unbalanced and distorted source voltages. Different filter structures and control strategies have been discussed in detail. Simulations have been provided for every control strategy and for all the different cases of disturbance in load.

Chapter 4 discusses the DSTATCOM in voltage control mode. Simulation results have been provided for all possible disturbances in the source and load.

Chapter 5 discusses the DVR. The theory of series compensation has been discussed. Two different filter structures have been discussed and have been simulated. Simulations have been presented for a deep sag in the source voltages.

CHAPTER 2

INVERTER TOPOLOGIES – A COMPARISON

Voltage Source Inverters (VSI) are used to realize a DSTATCOM or a DVR. The structure of the VSI decides the extent of compensation it can provide. For a particular type of distribution system a certain simple topology of VSI maybe sufficient but for others a more complex topology maybe required. For example in a simple three-phase four wire distribution system with a balanced source and balanced load the requirement maybe only to make the PCC at unity power factor or to maintain the load bus at a desired voltage. Hence in the case of a DSTATCOM the shunt injected currents will be balanced and in the case of a DVR the series injected voltages will be balanced. However, if in the above system either the source or the load was to be unbalanced or distorted the injected currents or voltages would also have to be unbalanced and distorted.

This chapter has been divided into two sections with the first and second section describing VSI topologies for DSTATCOM and DVR respectively. At the end of each section a comparison has been made between the inverter topologies and a particular topology selected as the best that will be used in further chapters. Simulation results have also been provided for comparison.

2.1 INVERTER TOPOLOGIES FOR A DSTATCOM

In the VSI structures the switches contain an Insulated Gate Bipolar Transistor (IGBT) with its associated anti-parallel diode. The energy storage device on the DC side of the inverter is a capacitor. Before discussing the inverter structures for DSTATCOM, the method of generating references for the compensator current is discussed.

2.1.1 Generation of Reference Currents for DSTATCOM

An algorithm had been formulated for generating the references for the compensator currents [8, 9, 14, 16] based on the method of instantaneous symmetrical components. A detailed discussion on real and reactive powers in a three-phase four-

wire system as well as the limitations of the algorithm has been carried out in the next chapter.

Since the source currents are required to be balanced,

$$i_{sa} + i_{sb} + i_{sc} = 0 \tag{2.1}$$

For the source currents to have a particular phase angle (ϕ) with respect to the source voltages,

$$\angle v_{sa1} = \angle i_{sa1} + \phi \tag{2.2}$$

where v_{sa1} and i_{sa1} are the positive sequence components of the source voltage and source current respectively and are given by

$$v_{sa1} = \frac{1}{\sqrt{3}}\left(v_{sa} + \alpha v_{sb} + \alpha^2 v_{sc}\right) \tag{2.3}$$

$$i_{sa1} = \frac{1}{\sqrt{3}}\left(i_{sa} + \alpha i_{sb} + \alpha^2 i_{sc}\right) \tag{2.4}$$

where $\alpha = e^{j2\pi/3}$

On simplifying the above expression, the following equation is obtained,

$$(v_{sb} - v_{sc} - 3\beta v_{sa})i_{sa} + (v_{sc} - v_{sa} - 3\beta v_{sb})i_{sb} + (v_{sa} - v_{sb} - 3\beta v_{sc})i_{sc} = 0 \tag{2.5}$$

Where $\beta = \dfrac{tan\phi}{\sqrt{3}}$

For the source currents to be pure sinusoids without any harmonics,

$$v_{sa}i_{sa} + v_{sb}i_{sb} + v_{sc}i_{sc} = p_{lav} \tag{2.6}$$

Where p_{lav} is the average load power obtained by feeding the instantaneous load power p_l to a moving average filter or a low pass filter.

Writing the above equations in a matrix form we get

$$\begin{bmatrix} 1 & 1 & 1 \\ v_{sb} - v_{sc} - 3\beta v_{sa} & v_{sc} - v_{sa} - 3\beta v_{sb} & v_{sa} - v_{sb} - 3\beta v_{sc} \\ v_{sa} & v_{sb} & v_{sc} \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ p_{lav} \end{bmatrix} \tag{2.7}$$

Hence the references for the compensator currents can be obtained by applying KCL at the PCC.

$$i_{fk}^{*} = i_{lk} - i_{sk} \tag{2.8}$$

where $k = a, b, c$

Solving Eqn (2.7) and substituting expressions for the source current in the Eqn (2.8) we get

$$\left.\begin{aligned} i_{fa}^{*} &= i_{la} - \frac{v_{sa} + (v_{sb} - v_{sc})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} p_{lav} \\ i_{fb}^{*} &= i_{lb} - \frac{v_{sb} + (v_{sc} - v_{sa})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} p_{lav} \\ i_{fc}^{*} &= i_{lc} - \frac{v_{sc} + (v_{sa} - v_{sb})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} p_{lav} \end{aligned}\right\} \quad (2.9)$$

Eqn (2.9) will be used to generate reference currents for the DSTATCOM for all simulations in this chapter.

2.1.2 Three Leg VSI with Single DC Storage Capacitor

Fig. 2.1 shows the circuit of the three-leg VSI with single DC storage capacitor [4, 11, 12, 13]. The operation of the switches S_1 to S_6 depends on the control strategy used. Some of the methods used to control the DSTATCOM are PWM current control, hysteresis current control, output feedback control or state feedback control. In this thesis report only the latter three control techniques have been discussed.

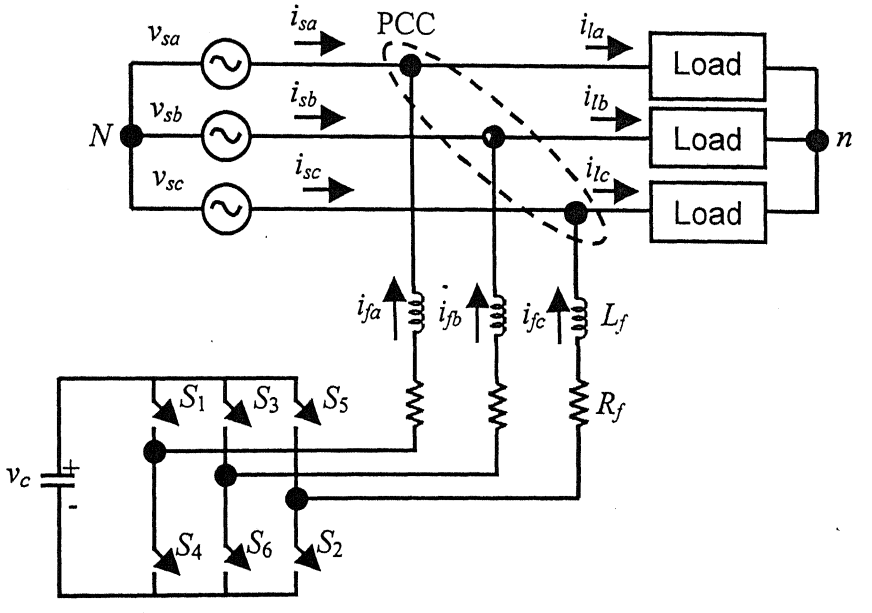

Fig. 2.1 DSTATCOM using three-leg VSI

The DSTATCOM using a three-phase three-leg inverter with single DC storage capacitor is capable of injecting currents such that

$$i_{fa} + i_{fb} + i_{fc} = 0 \tag{2.10}$$

Since there is no return path for the zero sequence component of current back to the inverter, the three-leg inverter with single DC storage capacitor cannot inject currents having a zero sequence component. From Fig. 2.1 it can be observed that the DSTATCOM has been connected to a three-phase three-wire system. There will be no zero sequence component in the load current irrespective of the load being balanced or unbalanced. If the load were to be unbalanced, the neutral voltage v_{nN} would oscillate and would not remain at zero which is not desirable. For a three-phase four wire systems with unbalanced loads, full compensation is not possible as the zero sequence component in the load current cannot be compensated. Hence, the DSTATCOM with the above topology of inverter can be used only for a three-phase three-wire system with balanced source voltages and balanced load currents and hence its application is somewhat limited.

The system parameters chosen for the simulation studies are listed in Table 2.1. Instead of the DC storage capacitor shown in Fig. 2.1 a DC battery is used.

Table 2.1 System Parameters

System Parameters	Values of Parameters
Source voltages	Balanced sinusoids with $V_{sa} = 6.3509\angle 0°$ kV
Load	Balanced passive load of $R_L + jX_L = 222.0+j125.66\ \Omega$
	Diode rectifier having a load of $R + jX = 150 + j12.56\ \Omega$
DSTATCOM	$V_{dc} = 25$ kV $R_f = 0.01\ \Omega$, $L_f = 40$ mH R_f represents the inverter losses.

In order to track the references for the compensator currents hysteresis current control method will be used for controlling the switching of the VSI that can be described in the following manner

If $i_{fa} - i_{fa}^* < -h$ then $S_1 = 1, S_4 = 0$

If $i_{fa} - i_{fa}^* > h$ then $S_1 = 0, S_4 = 1$

If $i_{fb} - i^*_{fb} < -h$ then $S_3 = 1, S_6 = 0$

If $i_{fb} - i^*_{fb} > h$ then $S_3 = 0, S_6 = 1$

If $i_{fc} - i^*_{fc} < -h$ then $S_5 = 1, S_2 = 0$

If $i_{fc} - i^*_{fc} > h$ then $S_5 = 0, S_2 = 1$

where h is the hysteresis band.

All simulation results in this thesis are obtained using PSCAD/EMTDC (Version 3.0.7). However the resulting data are transferred to MATLAB for plotting. Fig. 2.2 below shows the simulation results. Fig. 2.2 (a) shows the source voltages to be balanced sinusoids. Fig. 2.2 (b) shows the load currents to be distorted. Fig. 2.2 (c) shows the source currents to be balanced and sinusoidal due to the action of the compensator. However the source currents are seen to have a considerable amount of ripple. This is because a filter has not been used to remove the high frequency harmonic components in the compensator current that has been generated by the switching of the VSI from entering the system. The use of filters will be discussed in Chapter 3. Fig. 2.2 (d) shows the source voltage and the source current of phase A to be in phase with each other. Note that the source voltage has been scaled down by a factor of 20.

The simulation is repeated assuming that the passive load to be unbalanced as follows

$R_a + jX_a = 50 + j21.98\ \Omega$

$R_b + jX_b = 170 + j31.41\ \Omega$

$R_c + jX_c = 222 + j125.65\ \Omega$

The simulation results are shown in Fig. 2.3. From Fig. 2.3 (c) it can be seen that the source currents are neither balanced nor sinusoidal since full compensation has not been possible. However from Fig. 2.3 (d) it is evident that the source voltages and currents remain in phase due to the action of the compensator. Therefore the conclusion is that the compensator has failed.

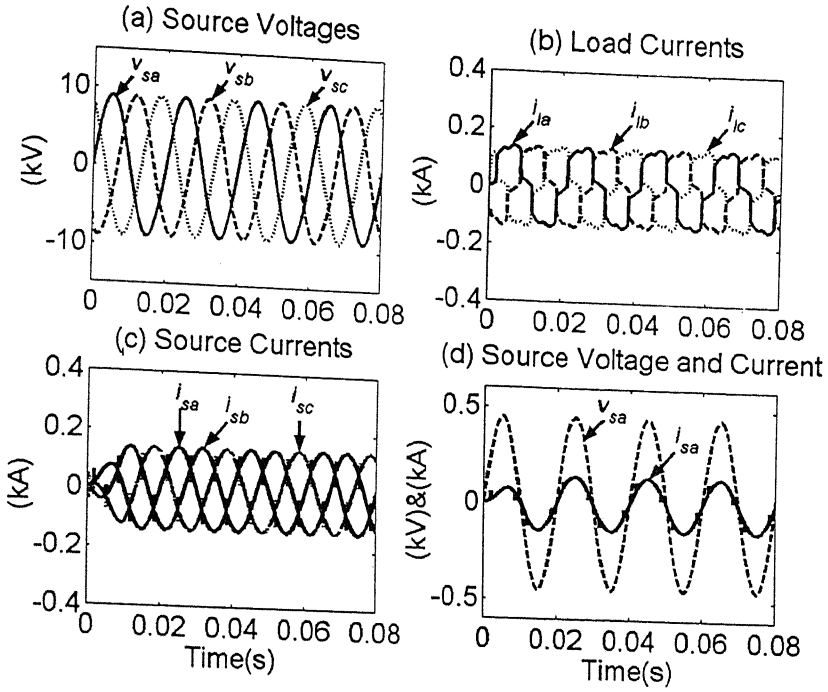

Fig. 2.2 Simulation of circuit in Fig. 2.1 considering balanced load

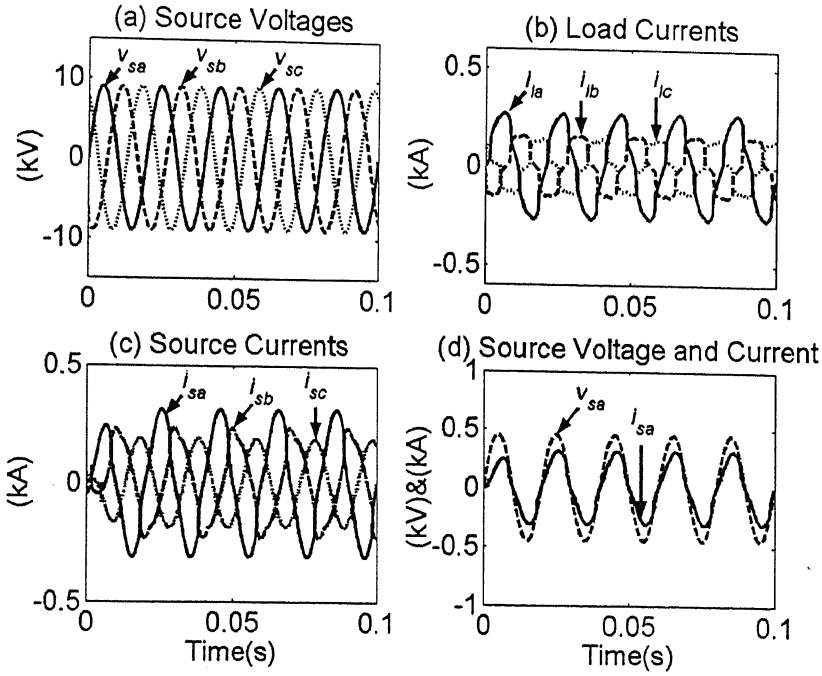

Fig. 2.3 Simulation of circuit in Fig. 2.1 considering unbalanced load

2.1.3 Three Independent Single Phase Inverters With Single DC Storage Capacitor

Fig. 2.4 shows the circuit of three single-phase inverters with a single DC storage capacitor [1, 9]. A transformer is connected to each single-phase inverter. As can be seen from the figure the inverter is used for three-phase four-wire systems since the neutral of the source (N), the neutral of the load (n) and the star point of the secondary windings of the transformer (n') are connected to each other. Hence there is a return path for the zero sequence component in the compensator current along the path (n-n').

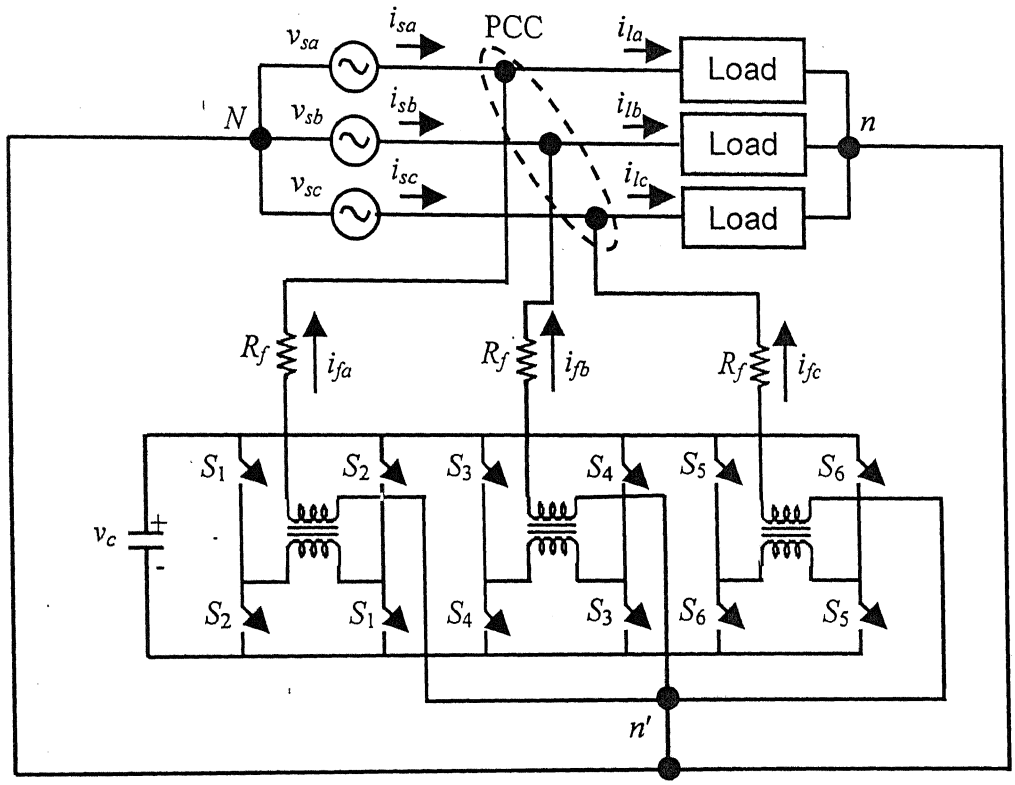

Fig. 2.4 DSTATCOM using three independent single-phase inverters with single DC storage capacitor

The transformers are essential in this topology and their absence will result in a short circuit of the DC storage capacitor as shown in Fig. 2.5. For example assume that the switches S_1, S_4 and S_5 are closed and the switches S_2, S_3 and S_6 are open. The dotted line indicates that the DC storage capacitor has been short-circuited. In the presence of the transformer, each single-phase inverter will be isolated from the other two.

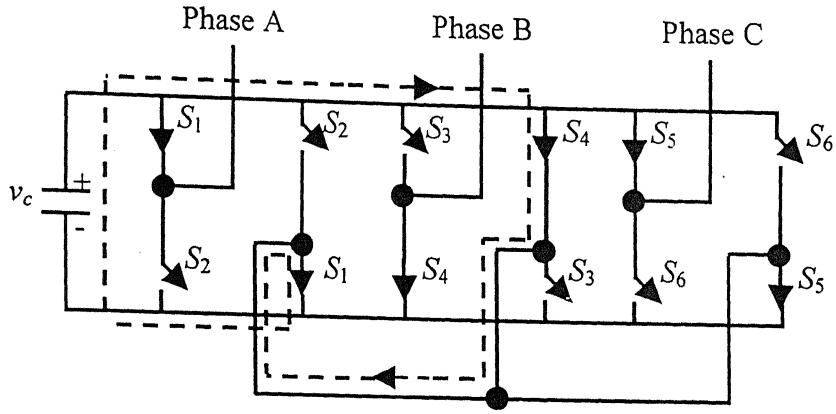

Fig. 2.5 Short-circuit of DC storage capacitor without isolation transformers

The system parameters chosen for the simulation are listed in Table 2.2. As before the simulation is performed with a DC battery instead of a DC storage capacitor.

Table 2.2

System Parameters	Values of Parameters
Source voltages	Balanced sinusoids with $V_{sa} = 6.3509\angle 0°$ kV
Load	Balanced passive load of $R_a + jX_a = 50 + j21.98\ \Omega$ $R_b + jX_b = 170 + j31.41\ \Omega$ $R_c + jX_c = 222 + j125.65\ \Omega$
	Diode rectifier having a load of $R + jX = 150 + j12.56\ \Omega$
DSTATCOM	$V_{dc} = 550$ V Transformer of 5 MVA, 440V/22kV with a leakage reactance of 10% $R_f = 0.01\ \Omega$ R_f represents the inverter losses.

In order to track the references for the compensator current hysteresis current control method is used to control the switching of the VSI that can be described in the following manner

If $i_{fa} - i_{fa}^* < -h$ then $S_1 = 1, S_2 = 0$

If $i_{fa} - i_{fa}^* > h$ then $S_1 = 0, S_2 = 1$

If $i_{fb} - i_{fb}^* < -h$ then $S_3 = 1, S_4 = 0$

If $i_{fb} - i_{fb}^{*} > h$ then $S_3 = 0, S_4 = 1$

If $i_{fc} - i_{fc}^{*} < -h$ then $S_5 = 1, S_6 = 0$

If $i_{fc} - i_{fc}^{*} > h$ then $S_5 = 0, S_6 = 1$

Fig. 2.6 shows the simulation results. The source currents are balanced sinusoids and in phase with the respective source voltages.

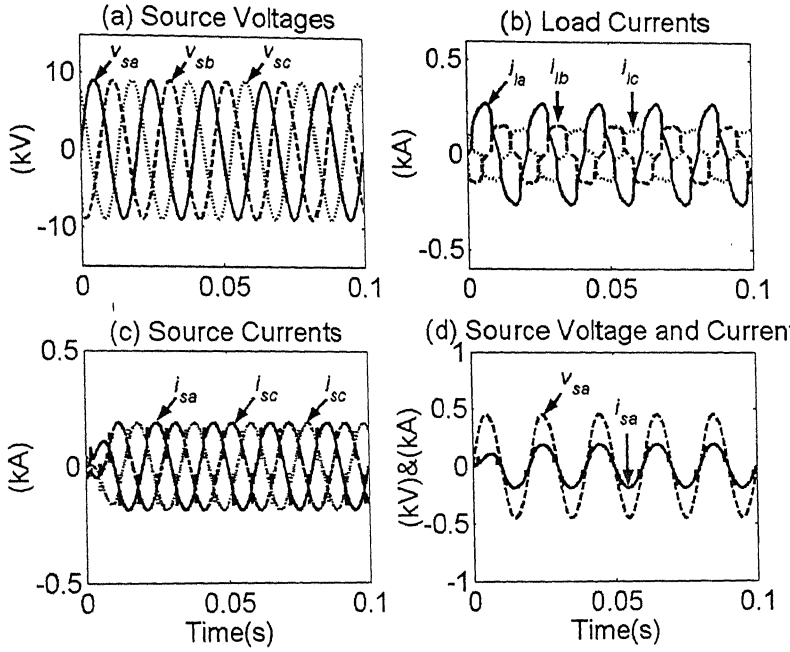

Fig. 2.6 Simulation of circuit in Fig. 2.4 considering unbalanced load

In certain cases the load may consist of half-wave rectifiers or unsymmetrical semi-converters that would result in a DC component in the load current. Such converters are used only for small loads. However in a distribution system it is possible that the widespread use of half-wave rectifiers or unsymmetrical semi-converters could result in an appreciable amount of DC component in the load current that cannot be neglected. A DC component can also result due to geomagnetic effect in countries close to the poles. Hence the compensator would also be required to supply a DC component for the phases where the load current contains a DC component. However due to the presence of the transformers the inverter cannot compensate DC components in the load current as the transformers would saturate. Hence this topology cannot be used for loads that might draw a current having a DC component.

2.1.4 Three Leg VSI With Neutral Clamped DC Storage Capacitor

Fig. 2.7 shows the circuit of the three-leg VSI with neutral clamped DC storage capacitor [1, 5]. This topology can be considered to be an alternative to the topology discussed in Section 2.1.2.

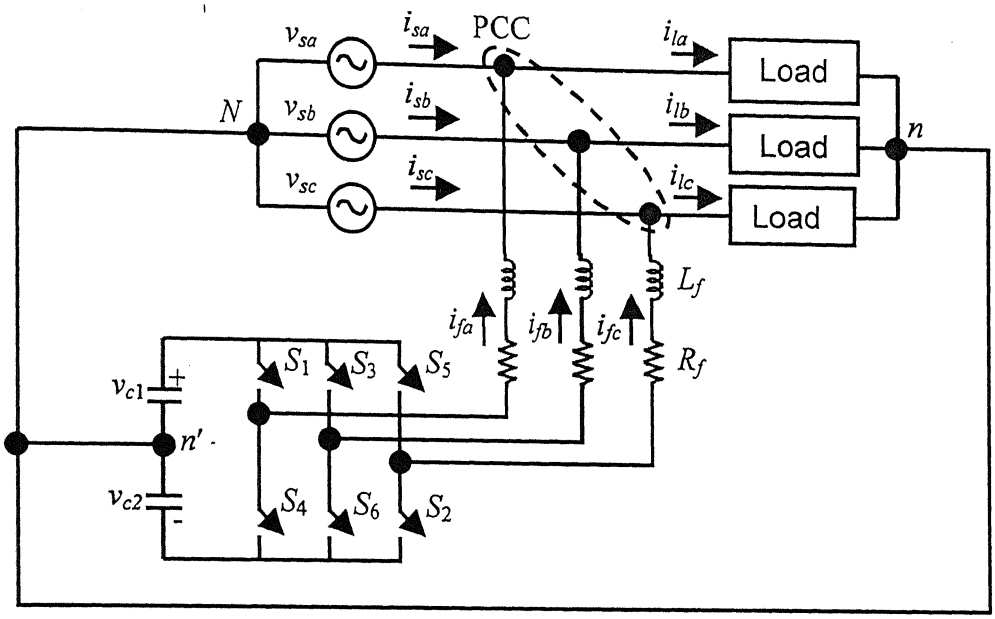

Fig. 2.7 DSTATCOM using three-leg VSI with neutral clamped DC storage capacitor

From Fig. 2.7 it can be observed that the DSTATCOM using the three-leg VSI with neutral clamped DC storage capacitor is used for a three-phase four wire-system. The neutral of the source (N), the neutral of the load (n) and the neutral of the DC capacitors (n') are connected together. If the load is unbalanced, the load current will have a zero sequence component and the compensator will be required to supply this zero sequence component. As there is a path n-n' for the zero sequence component to return to the compensator, the compensator will be able to compensate for unbalanced loads.

For simulation of the above circuit the system parameters chosen are listed in Table 2.3. In order to track the references for the compensator current hysteresis current control is used to control the switching of the VSI in a manner identical to the strategy employed for the three-leg inverter with single DC storage capacitor discussed in Section 2.1.2.

Table 2.3

System Parameters	Values of Parameters
Source voltages	Balanced sinusoids with $V_{sa} = 6.3509\angle 0°$ kV
Load	Balanced passive load of $R_a + jX_a = 50 + j21.98\ \Omega$ $R_b + jX_b = 170 + j31.41\ \Omega$ $R_c + jX_c = 222 + j125.65\ \Omega$
	Diode rectifier having a load of $R + jX = 150 + j12.56\ \Omega$
DSTATCOM	$V_{dc1} = 12.5$ kV, $V_{dc2} = 12.5$ kV $R_f = 0.01\ \Omega$, $L_f = 40$ mH R_f represents the inverter losses.

Fig. 2.8 shows the simulation results. The source currents are balanced sinusoids and in phase with the respective source voltages.

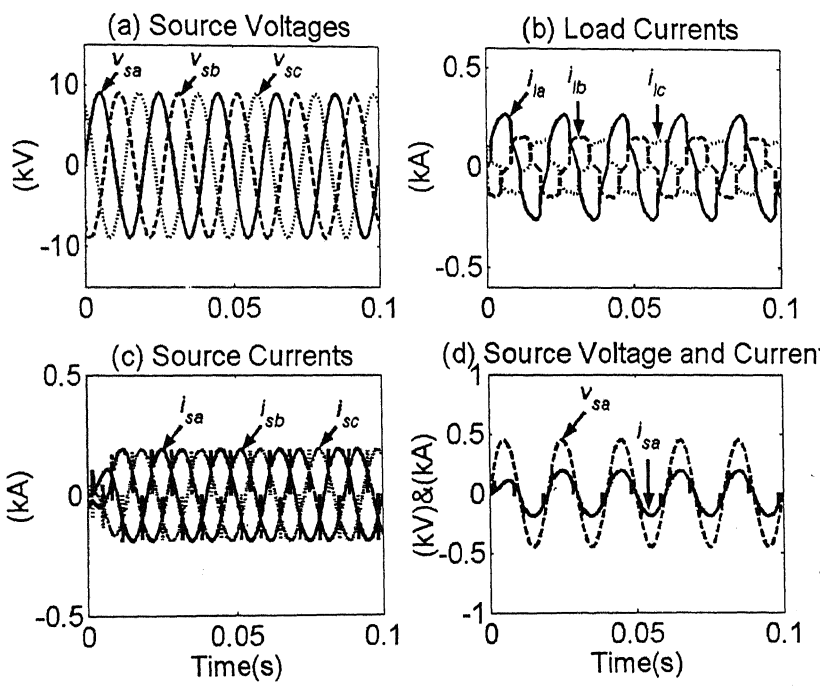

Fig. 2.8 Simulation of circuit in Fig. 2.7 considering unbalanced load

The zero sequence current flowing into the neutral point of the DC storage capacitors through the path *n-n'* will divide and flow into the capacitors causing a ripple in their voltage from the DC value of a frequency equal the frequency of the currents present in the zero sequence component. However as explained in Section 2.1.3 above,

in certain cases the load may consist of half-wave rectifiers or unsymmetrical semi-converters. Due to this the load current will have not only harmonics but also a DC component. This DC component in the load current will also flow through the path n-n'. At point n' the DC current will flow through the two DC storage capacitors causing the upper capacitor to discharge and the lower to charge. Hence the voltages of the DC storage capacitors will continuously drift. By using a PI controller the sum of the voltages of the DC storage capacitors is maintained at a constant value V_{dc} by controlling the power flow to the inverter from the system. However the voltages of each of the capacitors cannot be controlled individually. As time progresses the voltage of the discharging capacitor will fall to such an extent that the compensator will no longer be able to track the desired reference current. At this stage the voltages of the two capacitors will stabilize at their respective values.

To prevent the divergence of the voltages of the DC storage capacitors a chopper is used across the DC storage capacitors [9, 14] as shown in Fig. 2.9. The basic principle behind the working of the chopper is that it injects a current at the neutral point of the DC storage capacitors n' such that the voltages of the capacitors are equal. In order to do so the reference for the current i_{ch} to be injected at the node n' should be the average of the negative sum of the references for the three phase currents of the compensator. Hence only the DC component of the load current that appears at point n' will be compensated thereby limiting the bandwidth of the compensator. The triplen harmonics and fundamental frequency components in the zero sequence current that continue to flow through the DC storage capacitors will cause ripples of a small magnitude in their voltage which will not affect the tracking ability of the inverter. The three legs of the VSI connected to the PCC are controlled using hysteresis current control method in a manner identical to the control strategy used for the three-leg VSI with single DC storage capacitor discussed in Section 2.1.2.

In the Fig. 2.9 the voltages of the DC storage capacitors are denoted by v_{c1} and v_{c2}. By controlling the power flow to the inverter from the source, the sum of v_{c1} and v_{c2} is maintained at V_{dc}. The chopper should maintain the individual capacitor voltages at a voltage of $V_{dc}/2$. If the voltage v_{c1} rises above $V_{dc}/2$ and v_{c2} drops below $V_{dc}/2$, the switch S_7 is closed and the current i_{ch} increases storing energy in the inductor L_{ch} hence discharging the upper capacitor. The energy in the inductor then discharges through the anti-parallel diode across the switch S_8 thereby charging up the lower capacitor.

Similarly, when the upper capacitor voltage falls and the lower capacitor voltage rises the switch S_8 is closed and the energy in the inductor freewheels through the anti-parallel diode across S_7 to charge the upper capacitor.

Since the operation of the chopper prevents the divergence of the DC storage capacitors voltages and there is no need for isolation transformers the inverter can be used to compensate for loads drawing currents having a DC component.

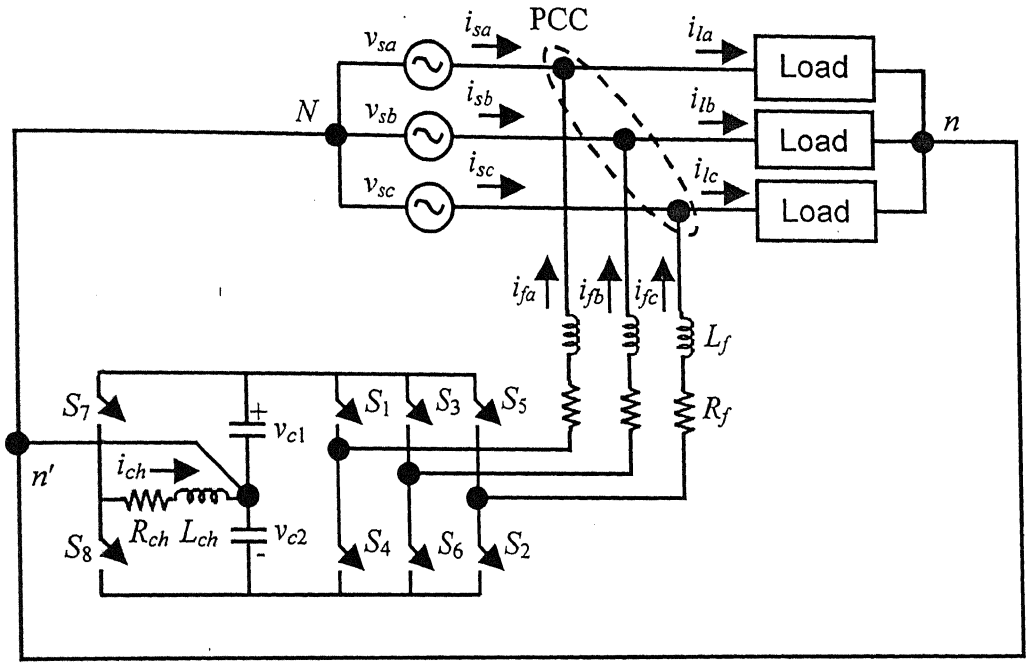

Fig. 2.9 DSTATCOM using three-leg VSI with neutral clamped DC capacitors controlled by a chopper

2.1.5 Three-Phase Four-Leg VSI

Fig. 2.10 shows the circuit of the three-phase four-leg VSI with a single DC storage capacitor [1, 5, 9]. This topology is applicable to three-phase four-wire systems. The load neutral (n) is connected to the source neutral (N) and also to the fourth leg of the inverter.

The reference for the current to be tracked by the fourth leg will be the negative sum of the three load currents

$$i_0^* = -(i_{la} + i_{lb} + i_{lc}) \tag{2.11}$$

This will contain the DC component, the zero sequence fundamental frequency components and triplen frequency components in the load current. Hence the bandwidth of the fourth leg would have to as large as that of the other three legs. As the

fourth leg can track the DC component in the load current and there is no need for isolation transformers, the inverter can compensate for loads drawing DC components. Since there is a single DC storage capacitor, the voltage across can be maintained by controlling the power flow through the inverter from the source.

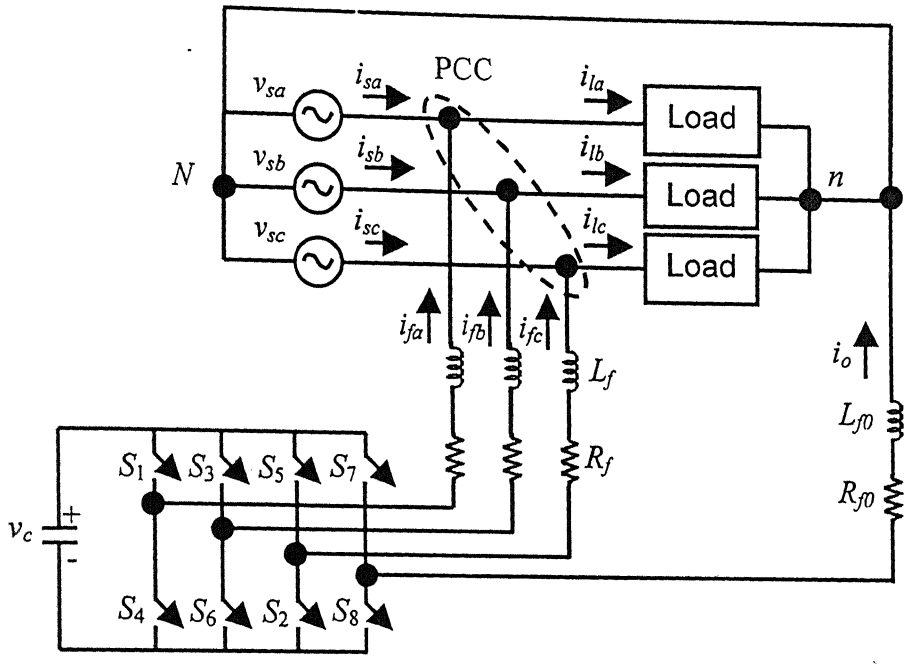

Fig. 2.10 DSTATCOM using four-leg VSI

The system parameters chosen for the simulation are listed in Table 2.4.

Table 2.4

System Parameters	Values of Parameters
Source voltages	Balanced sinusoids with $V_{sa} = 6.3509\angle 0°$ kV
Load	Balanced passive load of $R_a + jX_a = 50 + j21.98\ \Omega$ $R_b + jX_b = 170 + j31.41\ \Omega$ $R_c + jX_c = 222 + j125.65\ \Omega$
	Diode rectifier having a load of $R + jX = 150 + j12.56\ \Omega$
DSTATCOM	$V_{dc} = 25$ kV $R_f = 0.01\ \Omega$, $L_f = 40$ mH R_f represents the inverter losses.

Instead of a DC storage capacitor a DC battery is used for the simulation. The three legs connected to the PCC are controlled using hysteresis current control method

in the same manner used for the three-leg VSI with single DC storage capacitor discussed in Section 2.1.2. The fourth leg will also be controlled using hysteresis current control method as follows

If $i_0 - i_0^* < -h$ then $S_7 = 1, S_8 = 0$

If $i_0 - i_0^* > h$ then $S_7 = 0, S_8 = 1$

Fig. 2.11 shows the simulation results. The source currents are balanced sinusoids and in phase with the respective source voltages despite the load currents being unbalanced and distorted.

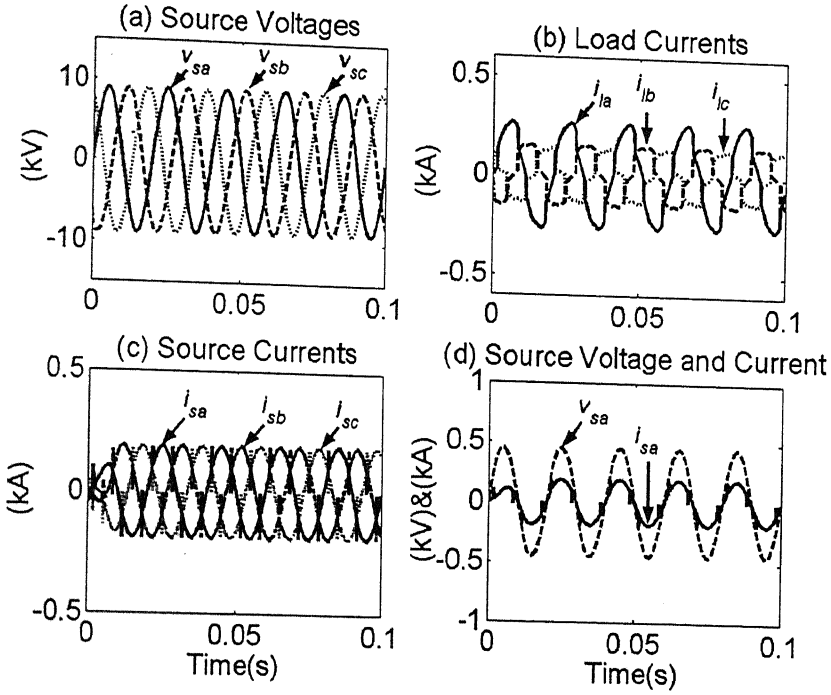

Fig. 2.11 Simulation of circuit in Fig. 2.10 considering symmetrical load

2.2 COMPARISON BETWEEN THE DSTATCOM TOPOLOGIES

In this section a comparison is made between the inverter topologies discussed from Section 2.1.2 to Section 2.1.5. The advantages and disadvantages of each topology will be discussed below.

Section 2.1.2 describes the topology of the three-phase three-leg inverter. This inverter cannot compensate unbalanced loads or loads which draw DC components or

triplen frequency components. Hence this inverter can be used in very limited applications.

Section 2.1.3 describes the topology of three single-phase inverters using a single DC storage capacitor. The major disadvantage of this topology is that the inverter uses twelve IGBTs and twelve anti-parallel diodes and it needs three isolation transformers. Though it can compensate for zero sequence components having fundamental frequency and triplen harmonics it cannot compensate for loads drawing a DC component in the load current. However the advantage of this topology is that if step-up isolation transformers are used the voltage across the DC storage capacitor will be low.

Section 2.1.4 describe the topology of the three-leg inverter with neutral clamped DC storage capacitors without and with a chopper. Due to the operation of the chopper the inverter is capable of compensating loads drawing any kind of current including zero sequence components of fundamental frequency, triplen harmonics as well as DC components The chopper prevents the divergence of the voltages even though it could be operated at a low frequency. However the chopper operation makes the control circuit very complex. This topology is superior to the topologies of inverters discussed in Sections 2.1.2 and Section 2.1.3. However in this topology two DC storage capacitors are needed.

Section 2.1.5 describes the topology of the four-leg inverter with a single DC storage capacitor. This topology is very close to the topology of the inverter having a chopper described in Section 2.1.4 in the sense that it has the same number of switches and is also capable of compensating currents having zero sequence components of fundamental frequency, triplen harmonics and DC components. The drawback of this inverter over the three-leg inverter with neutral clamped DC storage capacitors and chopper is that the fourth leg of the inverter must have the same bandwidth as the remaining three legs and will switch at approximately the same frequency as the other three legs. The advantage is that only one DC storage capacitor is required. The IGBTs used nowadays are capable of switching at frequencies of 20 kHz. Hence the appreciable switching frequency of the fourth leg does not cause any problem. However the DC storage capacitors in the inverters will be required to have a high voltage rating. Hence the use of a single capacitor instead of two capacitors is a considerable advantage. Due to the above reasons the four-leg inverter is used in further analysis.

2.3 INVERTER TOPOLOGIES FOR A DVR

The inverter topologies for the DVR are similar to the topologies discussed for the DSTATCOM above. Three inverter topologies along with their application to distribution systems are described below. A section is devoted to highlighting the advantages and disadvantages of the different topologies.

2.3.1 Three-Leg VSI

Fig. 2.12 shows the topology of the DVR using the three-leg VSI [12, 19]. The capacitor C_d that is connected across the secondary of the transformer acts as a filter to attenuate the high frequency switching ripples present in the output voltage of the inverter. The source in this system is balanced. Hence the DVR plays the role only of a voltage regulator in the event of sag and swell and can remove any distortion in the source voltages if they are balanced as well. In the case of unbalance in the source voltages the injected voltages must also be unbalanced. If the injected voltages must be unbalanced, the current injected by the inverter must also be unbalanced. In the Fig. 2.12, the star points of the primary terminals of the three transformers are connected together leaving no path for the zero sequence component of the injected currents to flow. Therefore the DVR cannot compensate for any unbalance in the source voltages.

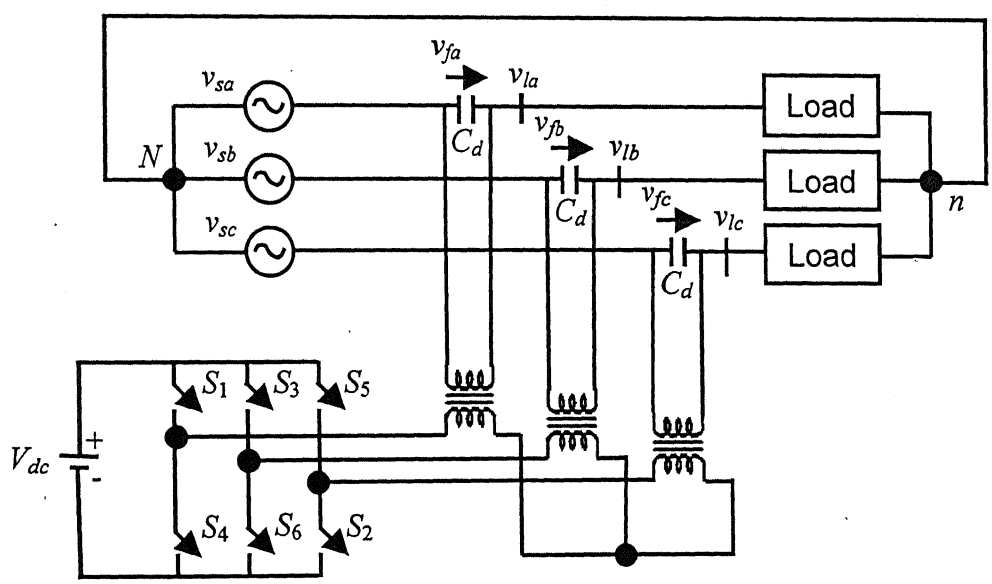

Fig. 2.12 DVR using three-leg VSI

Table 2.5 System Parameters

System Parameters	Values of Parameters
Source Voltages in kV	$v_{sa} = 9.0\sin(100\pi t) + 0.9\sin(5*(100\pi t)) + 0.42\sin(7*(100\pi t))$ $v_{sb} = 9.0\sin(100\pi t - 2\pi/3) + 0.9\sin(5*(100\pi t - 2\pi/3)) + 0.42\sin(7*(100\pi t - 2\pi/3))$ $v_{sc} = 9.0\sin(100\pi t + 2\pi/3) + 0.9\sin(5*(100\pi t + 2\pi/3)) + 0.42\sin(7*(100\pi t + 2\pi/3))$
Sensitive Load	$R + jX = 75 + j31.41$ ohm
DVR	$V_{dc} = 3$ kV 5 MVA, 3.3kV/22kV transformer with 10% leakage reactance Filter capacitor $C_d = 50\mu$F

The system parameters used for simulation are given in Table 2.5. It is desired that the load voltages are balanced sinusoids having a peak of 9kV. The simulation results are shown in Fig. 2.13. Fig. 2.13 (a) shows the source voltages are distorted but balanced as per Table 2.5 while the load voltages in Fig. 2.13(b) are balanced distortion free sinusoids having a peak of 9 kV.

To prove that the above topology for the DVR fails when it is required to inject voltages that are unbalanced, a magnitude unbalance in the fundamental components of the source voltages is considered as follows

$$v_{sa} = 9.0\sin(100\pi t) + 0.9\sin(5*(100\pi t)) + 0.42\sin(7*(100\pi t))$$

$$v_{sb} = 8.5\sin(100\pi t - 2\pi/3) + 0.9\sin(5*(100\pi t - 2\pi/3)) + 0.42\sin(7*(100\pi t - 2\pi/3))$$

$$v_{sc} = 9.5\sin(100\pi t + 2\pi/3) + 0.9\sin(5*(100\pi t + 2\pi/3)) + 0.42\sin(7*(100\pi t + 2\pi/3))$$

All the other system parameters remain the same as in Table 2.5. Fig. 2.14 shows the simulation results. Fig. 2.14(a) shows the source voltages are unbalanced and distorted. Fig. 2.14(b) shows that the load voltages are neither balanced nor sinusoidal as the DVR has not been able to inject the required voltages. A larger unbalance in the source voltages would make the load voltages even more unbalanced and distorted.

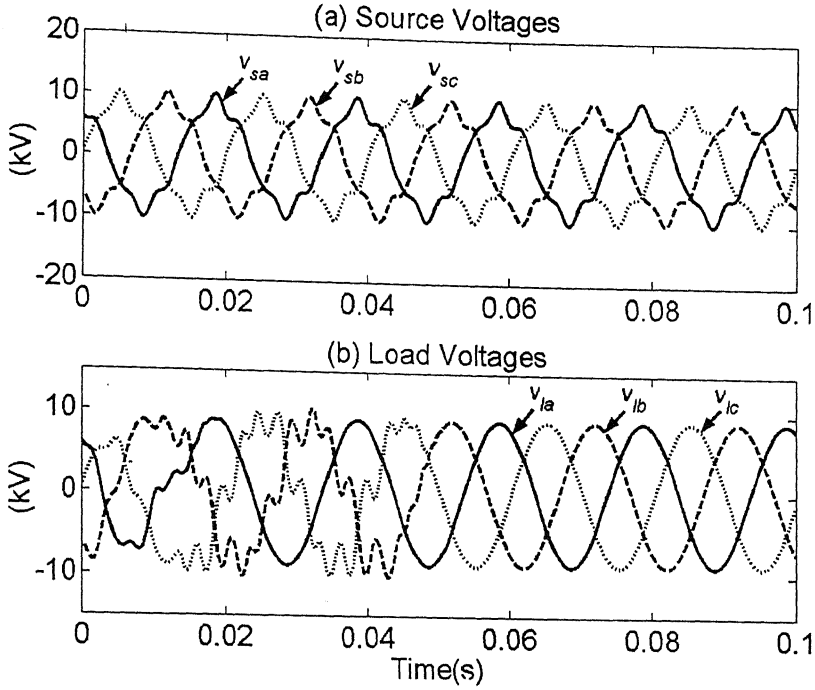

Fig. 2.13 Simulation of circuit in Fig. 2.12 considering balanced source voltages

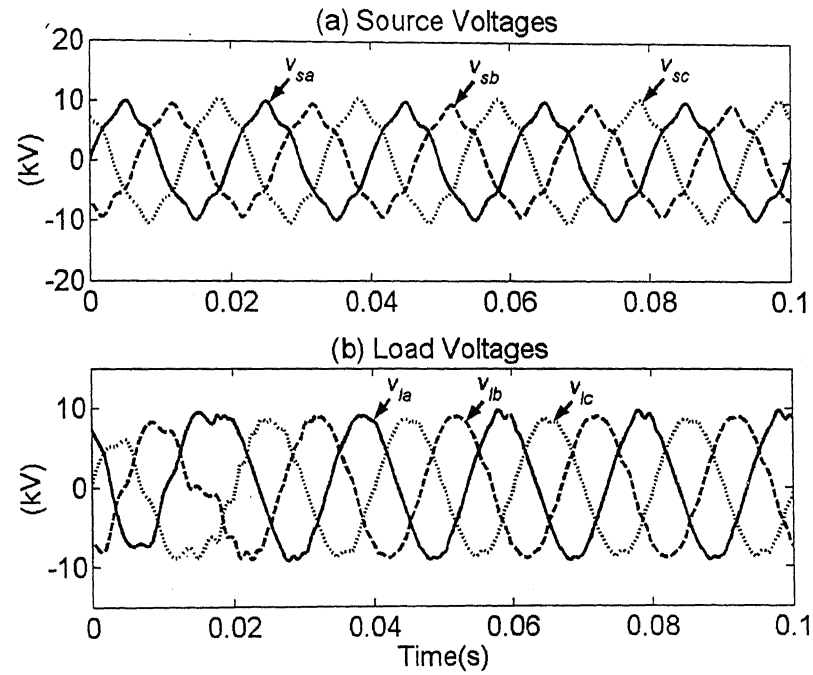

Fig. 2.14 Simulation of Fig. 2.12 considering unbalanced source voltages

2.3.2 Three Single-Phase Inverters with a Single DC Storage Capacitor

Fig. 2.15 shows the circuit diagram of three single-phase inverters with a single DC storage capacitor [9, 18, 23]. In this particular topology, each inverter is independent. Hence there is no restriction on the voltages that the DVR using this structure can inject. Each single-phase inverter provides a return path for the current to be injected and no separate path for the zero sequence component is required. Therefore the above structure can be used to compensate for source voltages that are unbalanced and distorted.

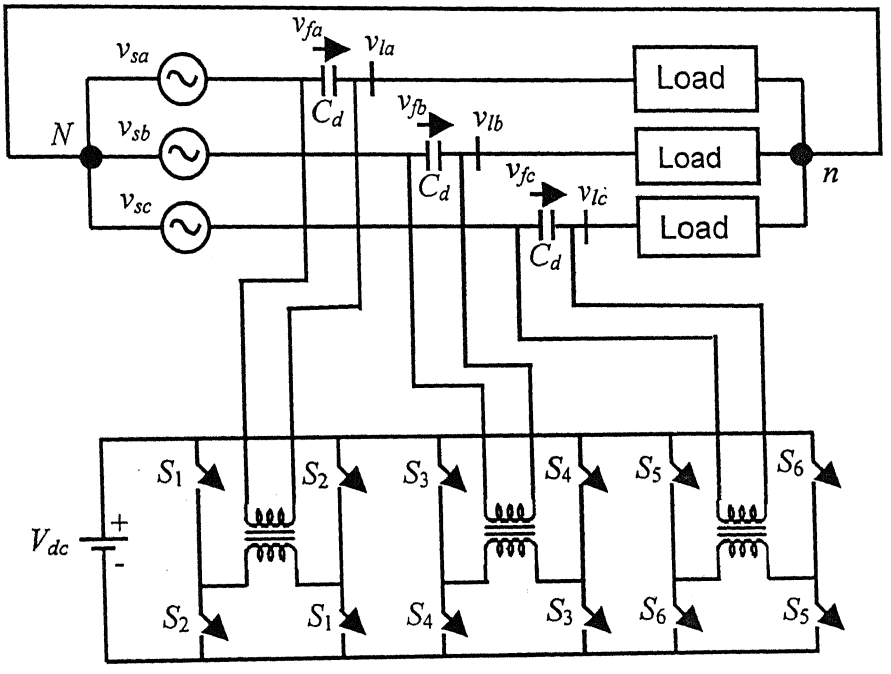

Fig. 2.15 DVR using three independent single-phase inverters with single DC storage capacitor

Considering the source voltages to be unbalanced and other system parameters as given in Table 2.5 a simulation is performed with this topology. Fig. 2.16 shows the simulation results. The load voltages are balanced sinusoids and have a peak of 9 kV though the source voltages are unbalanced and distorted.

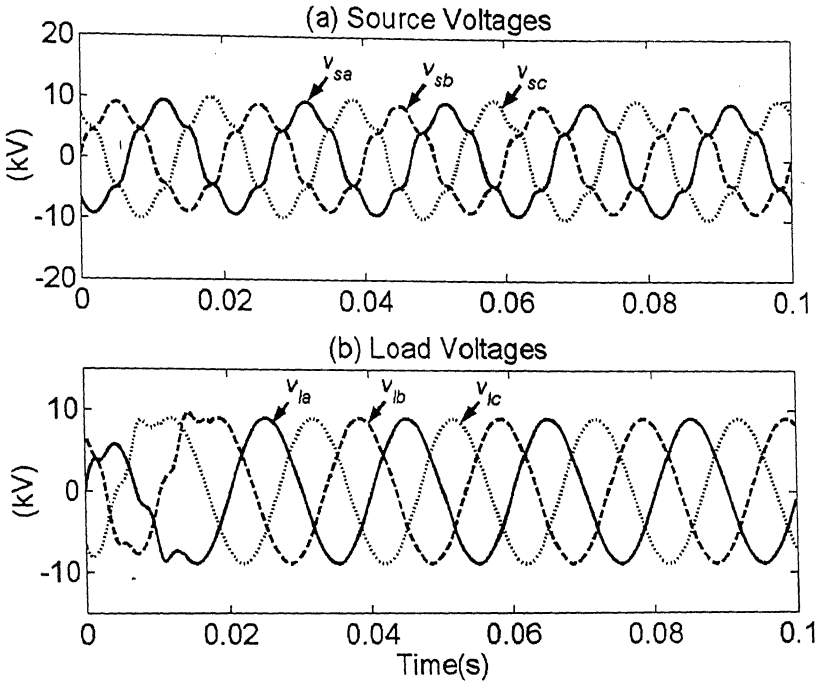

Fig. 2.16 Simulation of circuit in Fig. 2.15 considering unbalanced source voltages

2.3.3 Four-Leg VSI

Fig. 2.17 shows the circuit diagram of the four-leg VSI as a DVR. In this case the fourth leg of the VSI is connected to the star point of the transformer primary terminals. This fourth leg is made to track the negative sum of the references for the injected currents in the three phases. Hence a path is available for the zero sequence of the injected currents in the primaries of the transformers. This enables the VSI to inject unbalanced and distorted voltages.

For simulating the circuit of Fig. 2.17 the system parameters are considered to be the same as in the simulation in the Section 2.3.2. Fig. 2.18 shows the simulation results. The results are similar to the results in Fig. 2.16 for the DVR using three single-phase inverters with single DC battery.

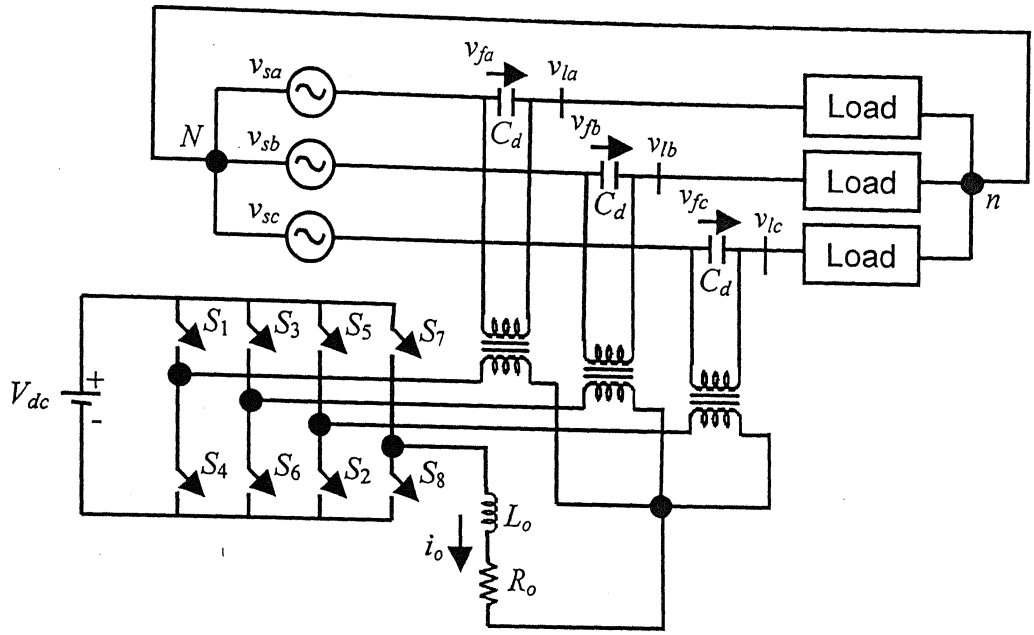

Fig. 2.17 DVR using four-leg VSI

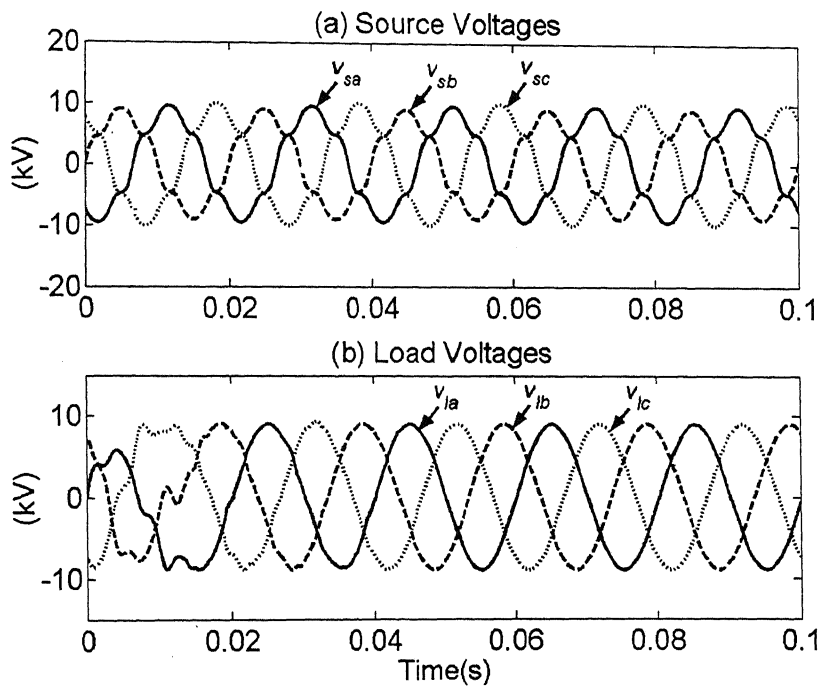

Fig. 2.18 Simulation of circuit in Fig. 2.17 considering unbalanced source voltages

2.4 COMPARISON BETWEEN THE DVR TOPOLOGIES

This section outlines the advantages and disadvantages of the inverter topologies for the DVR described in Section 2.3.1 to2.3.3. The inverter topology finally selected must be able to compensate for any condition of source voltages. Hence the DVR must be able to inject unbalanced as well as distorted voltages.

The three-leg inverter described in Section 2.3.1 cannot compensate for unbalance in the source voltages and is not suitable as a DVR structure. The three single-phase inverters with single DC storage capacitor described in Section 2.3.2 is capable of compensating for unbalanced and distorted source voltages. However it uses twelve IGBTs and twelve anti-parallel diodes which is the only disadvantage. The four-leg VSI described in Section 2.3.3 is capable of compensating for unbalanced and distorted source voltages as well. The advantage is that it needs only eight IGBTs and eight anti-parallel diodes. This topology will be used for simulation of the DVR in Chapter 5.

CHAPTER 3

DSTATCOM IN CURRENT-CONTROL MODE

In the previous chapter the various inverter topologies for the DSTATCOM have been discussed. In the current control mode, the objective of the DSTATCOM is to make the source currents balanced sinusoids and at a desired phase angle with respect to the source voltages. The chapter will begin with a basic discussion on the instantaneous real and reactive powers in a system and will continue to discuss an algorithm for filtering out the harmonics in the load current thereby ensuring that the source currents are balanced sinusoids and the source power factor is at any desired value. The drawbacks of the algorithm will be stated and a new algorithm will be proposed for overcoming this drawback.

The algorithms will be then applied to a DSTATCOM using a three-phase four-leg inverter with a DC battery described in Section 2.1.4 in chapter 2. Various control strategies for switching the inverter will be discussed and compared. The DC battery will be replaced by a DC storage capacitor and the method to maintain the voltage of the DC storage capacitor at the reference value will be discussed.

3.1 BASIC DEFINITIONS OF ACTIVE AND REACTIVE POWER

Consider a three phase four-wire system as shown in Fig. 3.1. In the derivations to follow the following conventions will be followed. The subscripts 'a', 'b' and 'c' denote the respective phases. Instantaneous quantities will be represented in lower case, vectors of instantaneous quantities will be represented in lower case bold letters. RMS phasors will be denoted by upper case letters and vectors of RMS phasors will be denoted by upper case bold.

The instantaneous active power is given by the scalar product between the vectors v and i as follows [6, 7, 9],

$$p = \boldsymbol{v}.\boldsymbol{i} = v_a i_a + v_b i_b + v_c i_c \tag{3.1}$$

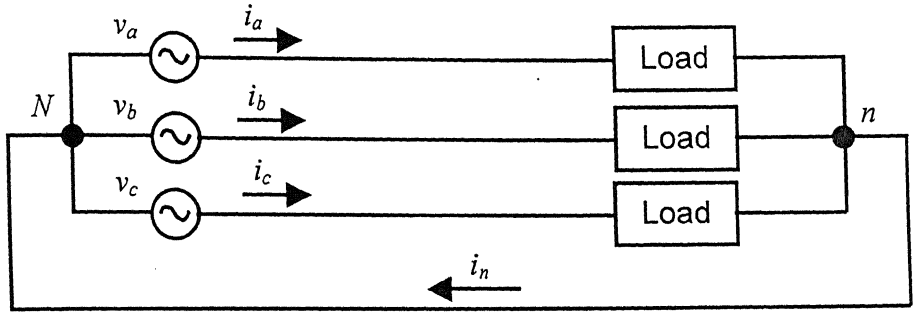

Fig. 3.1 Three-phase four-wire system

The instantaneous reactive power is given by the vector product between the vectors v and i as follows [6, 7, 9],

$$\boldsymbol{q} = \boldsymbol{v} \times \boldsymbol{i} = \begin{bmatrix} \begin{vmatrix} v_b & v_c \\ i_b & i_c \end{vmatrix} \\ \begin{vmatrix} v_c & v_a \\ i_c & i_a \end{vmatrix} \\ \begin{vmatrix} v_a & v_b \\ i_a & i_b \end{vmatrix} \end{bmatrix} \tag{3.2}$$

The instantaneous current and voltage vectors can be represented in terms of their sequence components as follows,

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \begin{bmatrix} v_{a0} \\ v_{a1} \\ v_{a2} \end{bmatrix} \tag{3.3}$$

$$\boldsymbol{v}_{abc} = \boldsymbol{P}\boldsymbol{v}_{012} \tag{3.4}$$

where $\alpha = e^{j2\pi/3}$

$$\boldsymbol{v}_{abc}^T = \begin{bmatrix} v_a & v_b & v_c \end{bmatrix}$$

$$\boldsymbol{v}_{012}^T = \begin{bmatrix} v_{a0} & v_{a1} & v_{a2} \end{bmatrix}$$

$$\boldsymbol{P} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix}$$

Similarly,

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \begin{bmatrix} i_{a0} \\ i_{a1} \\ i_{a2} \end{bmatrix} \tag{3.5}$$

$$\boldsymbol{i}_{abc} = \boldsymbol{P}\boldsymbol{i}_{012} \tag{3.6}$$

Using the Eqns (3.1), (3.3) and (3.5) above, the instantaneous active and reactive powers can be expressed in terms of the sequence components of voltage and currents as follows,

$$p = v_{a0}i_{a0} + v_{a2}i_{a1} + v_{a1}i_{a2} \tag{3.7}$$

For the instantaneous sequence components, the following relations hold at every instant of time

$$v_{a1} = v_{a2}^*, \; i_{a1} = i_{a2}^*$$

Therefore, $p = v_{a0}i_{a0} + \mathrm{Re}\left(v_{a1}i_{a1}^*\right)$ (3.8)

Similarly, the reactive power can be expressed as follows,

$$\boldsymbol{q} = \begin{bmatrix} q_a \\ q_b \\ q_c \end{bmatrix} = -\frac{2}{\sqrt{3}} \mathrm{Im} \begin{bmatrix} v_{a1}i_{a1}^* \\ v_{a1}i_{a1}^* \\ v_{a1}i_{a1}^* \end{bmatrix} - \frac{2}{\sqrt{3}} v_{a0} \mathrm{Im} \begin{bmatrix} i_{a1} \\ i_{a1}e^{-j2\pi/3} \\ i_{a1}e^{+j2\pi/3} \end{bmatrix} + \frac{2}{\sqrt{3}} i_{a0} \mathrm{Im} \begin{bmatrix} v_{a1} \\ v_{a1}e^{-j2\pi/3} \\ v_{a1}e^{+j2\pi/3} \end{bmatrix} \tag{3.9}$$

In a system in which the source voltages are perfectly balanced and sinusoidal,

$$v_{a0} = 0$$

Hence Eqn (3.8) reduces to,

$$p = \mathrm{Re}\left(v_{a1}i_{a1}^*\right) \tag{3.10}$$

The load is assumed to draw an unbalanced current containing harmonics. Hence the instantaneous active power can be resolved into two components – an average component indicated by an over bar and an oscillating component indicated by a tilde (~)

$$p = \bar{p} + \tilde{p} \tag{3.11}$$

For the instantaneous reactive power a summation of the instantaneous phase reactive powers can be defined which can be further resolved into an average component and an oscillating component as

$$q_{sum} = q_a + q_b + q_c = -2\sqrt{3}\,\mathrm{Im}\left(v_{a1} i_{a1}^{*}\right) \tag{3.12}$$

$$q_{sum} = \bar{q}_{sum} + \tilde{q}_{sum} \tag{3.13}$$

On the basis of the results derived above, the theory of shunt compensation will now be discussed.

3.2 THEORY OF SHUNT COMPENSATION

Fig. 3.2 shows the single-phase schematic diagram of a shunt compensator connected to a distribution system. The shunt compensator is depicted as an ideal current source. The source voltages as before are considered to be balanced sinusoids but the load is assumed to be drawing an unbalanced and distorted current.

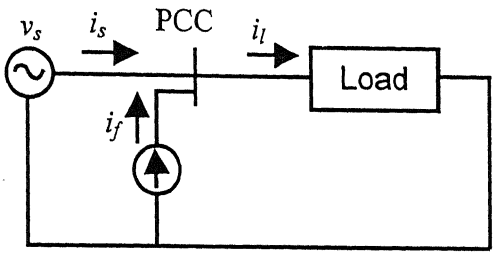

Fig. 3.2 Ideal compensator in shunt with a three-phase four-wire system

From Eqn (3.11), the instantaneous active load power (p_l) for the above diagram can be written as,

$$p_l = \bar{p}_l + \tilde{p}_l \tag{3.14}$$

From Eqn (3.13) the instantaneous load reactive power (q_{lsum}) can be written as,

$$q_{lsun} = \bar{q}_{lsum} + \tilde{q}_{lsum} \tag{3.15}$$

The objectives of shunt compensation are as follows

- The compensator must not supply any average real power to the load, i.e, the average load power must be equal to the power supplied by the source.
- The source must supply at the most a part of the reactive power demand of the load.

From the above two requirements the following relations can be written for the instantaneous source active and reactive powers [7, 9],

$$p_s = \bar{p}_l \tag{3.16}$$

$$q_{ssum} = \gamma \bar{q}_{lsum} \tag{3.17}$$

Where γ is a factor between –1 and 1. When γ is zero the source currents are in phase with the source voltages, when γ is positive the source currents lag the source voltages and when γ is negative the source currents lead the source voltages.

3.3 GENERATING REFERENCE COMPENSATOR CURRENTS USING INSTANTANEOUS SYMMETRICAL COMPONENTS

The two conditions given in the previous section along with the stipulation that the source current must not contain any negative sequence zero sequence or harmonic component leads to the algorithm for generating the references for the compensator currents that has already been derived in Section 2.1.1 of Chapter 2 [8, 9, 14, 16]. The equations are rewritten below for ready reference.

$$\left.\begin{aligned} i_{fa}^{*} &= i_{la} - \frac{v_{sa} + (v_{sb} - v_{sc})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} p_{lav} \\ i_{fb}^{*} &= i_{lb} - \frac{v_{sb} + (v_{sc} - v_{sa})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} p_{lav} \\ i_{fc}^{*} &= i_{lc} - \frac{v_{sc} + (v_{sa} - v_{sb})\beta}{v_{sa}^2 + v_{sb}^2 + v_{sc}^2} p_{lav} \end{aligned}\right\} \tag{3.18}$$

The factor β can be written in terms of the factor γ in Eqn (3.17) as follows

$$\beta = \frac{\gamma q_{lav}}{3 p_{lav}}$$

where q_{lav} is the average of the sum of the three per phase reactive powers given by Eqn. (3.12). The limitation of the above expressions for generating references for the compensator currents will be demonstrated by the simulations presented below.

3.3.1 Simulation of an Ideal Compensator with a Stiff Balanced Source

A source is called stiff because the feeder impedance between the source and the PCC is zero. Table 3.1 shows the parameters for the system chosen for the

simulation. Fig 3.3 shows the simulation results. In the simulation the source is required to be at unity power factor.

Table 3.1 System Parameters

System Parameters	Values of Parameters
Source Voltages	$V_{san} = 6.3509\angle 0°$ kV $V_{sbn} = 6.3509\angle -120°$ kV $V_{scn} = 6.3509\angle +120°$ kV
Load	Passive R-L load as follows Z_a = 50+j21.98 ohm Z_b = 170+j31.41 ohm Zc = 222+j125.64 ohm
	Diode rectifier having the following RL load at its output Z_L = 150+j12.56 ohm

Fig 3.3 (a) and (b) show the source voltages and load currents respectively. The load currents are seen to be unbalanced due to the unbalanced passive load and are distorted due to the diode rectifier with RL load. In the absence of any compensation the source currents would be the same as the load currents. Fig 3.3 (c) shows the source currents that are balanced sinusoids due to the action of the compensator. Fig 3.3 (d) shows the source current and source voltage of phase A to be in phase. Note that the source voltage has been scaled down by a factor of 15. Fig 3.3 (e) and (f) show the instantaneous active and reactive powers respectively. It can be seen that although the load draws a fluctuating power with non-zero mean, the source supplies a constant power equal to the mean of the load power because the compensator supplies an oscillating power having zero mean. Furthermore, the compensator is seen to be supplying the complete instantaneous load reactive power while the source is supplying zero reactive power. In all the graphs a half-cycle delay of 10 ms is observed for the system to become stable. This is because the moving average filter used to obtain the average load power p_{lav} from the instantaneous load power p_l performs averaging over a half-cycle and will supply a steady value only after a half-cycle.

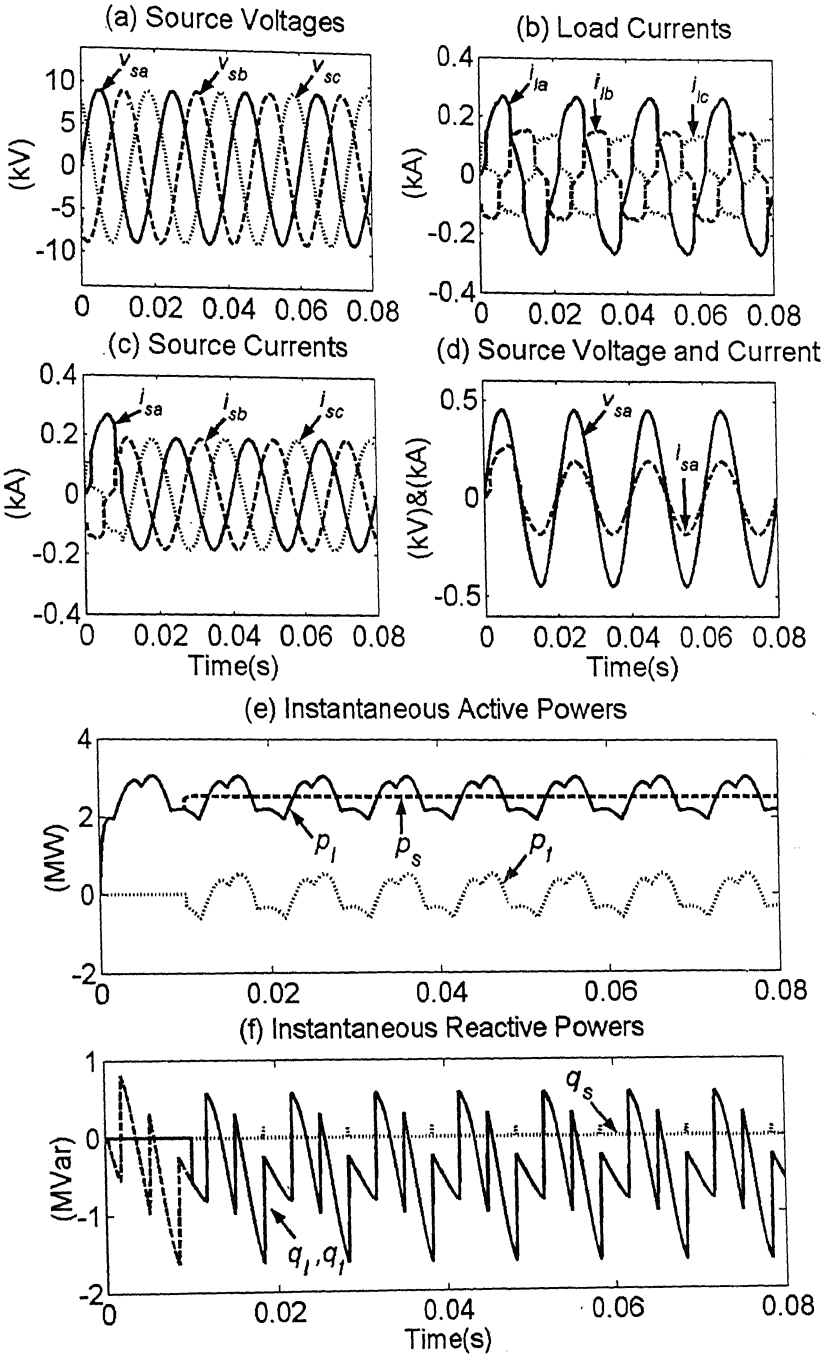

Fig. 3.3 System response with a DSTATCOM in the case of balanced sinusoidal source voltages

3.3.2 Simulation of an Ideal Compensator with a Stiff Unbalanced Source

The simulation of Section 3.3 is repeated with all the load parameters given in Table 3.1 remaining the same except for the source voltages in kV that are as follows

$$v_{sa} = 8.0\sin(100 * \pi t)$$

$$v_{sb} = 9.0\sin(100 * \pi t - 2\pi/3 - \pi/10)$$

$$v_{sc} = 10\sin(100 * \pi t + 2\pi/3 + \pi/10)$$

Fig 3.4 shows the simulation results. Fig 3.4 (a) shows the unbalanced source voltages. Fig 3.4 (b) shows that despite the operation of the ideal compensator the source currents are not balanced sinusoids. However from Fig 3.4 (c) and (d) it is observed that the compensator supplies the entire load reactive power and the oscillating load real power as the source reactive power is zero and the source real power is equal to the mean of the load reactive power. When the source voltages are balanced sinusoids, the compensator is able to meet the constraints $p_s = p_{lav}$ and $q_s = 0$ at the same time maintaining the source currents to be balanced sinusoids by injecting currents given by Eqn (3.18). However when the source voltages are unbalanced or if they were to be distorted as well, the algorithm in Eqn (3.18) fails to make the source currents balanced sinusoids. Hence for source voltages that may not be balanced sinusoids an alternate algorithm has been proposed in the next section.

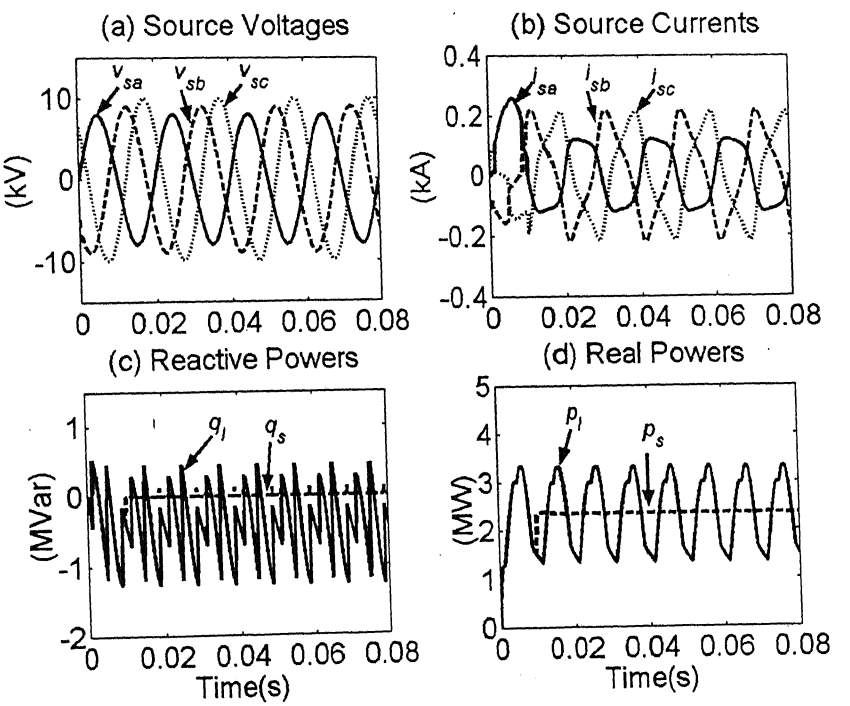

Fig. 3.4 System response with DSTATCOM in the case unbalanced sinusoidal source voltages

3.4 GENERATING REFERENCE COMPENSATOR CURRENTS USING PHASOR SYMMETRICAL COMPONENTS

All the sections above describe systems having stiff sources or in other words sources with no feeder impedance. Consider a system in which the source has a feeder with a non-negligible impedance as shown in Fig. 3.5. Hence the objective of shunt compensation would be to make the source currents balanced sinusoids and having a desired angle vis-à-vis to the PCC voltages.

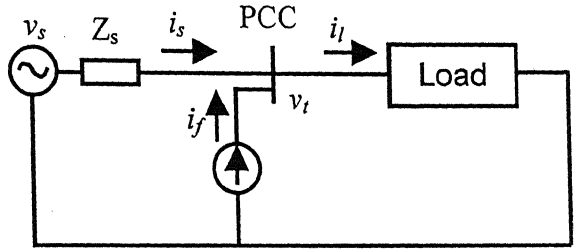

Fig. 3.5 Ideal compensator in shunt with a three-phase four-wire system having a non-stiff source

The instantaneous terminal voltages can be represented as

$$v_{tk} = v_{tkf} + \sum_{h=2,3,\ldots}^{\infty} v_{tkh} \tag{3.19}$$

where $k = a, b, c$.

The subscript f denotes the fundamental component of the terminal voltage while the subscript h denotes the harmonic contents of the terminal voltage and the number assigned to it is the harmonic number. If the terminal voltage were to be distorted in this manner, the fundamental can be extracted using an algorithm based on the following integral [9].

$$V_{tkf} = \frac{\sqrt{2}}{T} \int_T v_{tk} e^{-j(\omega t - \pi/2)} dt \tag{3.20}$$

where $\omega = 2\pi f$ and f is the base frequency of the system which in our case is 50Hz. In the above expression 'T' denotes the time interval of integration. In the case the signal contains only odd harmonics, T can be chosen to be half a cycle otherwise T will be full cycle. Integration is performed using a moving average calculation using latest samples.

When applied to all three phases Eqn (3.20) will provide phasors of the three fundamental PCC voltages (V_{tf}) that be written as

$$\left.\begin{aligned} V_{taf} &= V_{tafm}\angle\theta_a \\ V_{tbf} &= V_{tbfm}\angle(\theta_b) \\ V_{tcf} &= V_{tcfm}\angle(\theta_c) \end{aligned}\right\} \tag{3.21}$$

The above unbalanced phasors can be resolved into symmetrical components as follows

$$\begin{bmatrix} V_{taf0} \\ V_{taf1} \\ V_{taf2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_{taf} \\ V_{tbf} \\ V_{tcf} \end{bmatrix} \tag{3.22}$$

Similarly, the source currents can be resolved into symmetrical components

$$\begin{bmatrix} I_{sa0} \\ I_{sa1} \\ I_{sa2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_{sa} \\ I_{sb} \\ I_{sc} \end{bmatrix} \tag{3.23}$$

Since the source currents are required to be balanced sinusoids, the phasor symmetrical component of the source currents will give only a positive sequence component while the negative sequence and zero sequence component will be zero. i.e.,

$$I_{sa2} = 0$$
$$I_{sa0} = 0$$

The total three-phase power in terms of R.M.S phasors is given by [9]

$$P_{abc} + jQ_{abc} = V_{taf0}I^*_{sa0} + V_{taf1}I^*_{sa1} + V_{taf2}I^*_{sa2} \tag{3.24}$$

Now since $I_{as0} = I_{as2} = 0$

$$P_{abc} + jQ_{abc} = V_{taf1}I^*_{sa1} \tag{3.25}$$

This means

$$P_{abc} = |V_{taf1}||I_{sa1}|\cos(\phi) \tag{3.26}$$

$$Q_{abc} = |V_{taf1}||I_{sa1}|\sin(\phi) \tag{3.27}$$

where ϕ is the desired phase angle between the fundamental positive sequence of the PCC voltages and the source currents. Since the compensator must not supply any real power we have

$$P_{abc} = V_{taf1} I_{sa1} \cos(\phi) = p_{lav} \tag{3.28}$$

where p_{lav} is the average component of the instantaneous load power p_l obtained from a moving average filter as before. Therefore,

$$|I_{sa1}| = \frac{p_{lav}}{|V_{taf1}| \cos(\phi)} \tag{3.29}$$

The actual source current phasors are obtained by inverse transform,

$$\begin{bmatrix} I_{sa} \\ I_{sb} \\ I_{sc} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} 0 \\ I_{sa1} \\ 0 \end{bmatrix} = \begin{bmatrix} I_{sm} \angle \psi \\ I_{sm} \angle (\psi - 2\pi/3) \\ I_{sm} \angle (\psi + 2\pi/3) \end{bmatrix} \tag{3.30}$$

Hence the references for the instantaneous compensator current can be given by

$$\left.\begin{aligned} i_{fa} &= i_{la} - \sqrt{2} I_{sm} \sin(\omega t + \psi) \\ i_{fb} &= i_{lb} - \sqrt{2} I_{sm} \sin(\omega t - 2\pi/3 + \psi) \\ i_{fc} &= i_{lc} - \sqrt{2} I_{sm} \sin(\omega t + 2\pi/3 + \psi) \end{aligned}\right\} \tag{3.31}$$

3.5 CONTROL STRATEGIES FOR THE DSTATCOM

In this section, the various control strategies for the DSTATCOM are discussed with respect to the three-phase four-leg VSI topology presented in Section 2.1.4 of Chapter 2. Two different filter structures are considered to bypass the switching frequency components and improve the source current waveform. The expressions in Eqn. (3.31) will be used for generating references for compensator currents henceforth.

3.5.1 DSTATCOM Using Hysteresis Current Control Method

This section will describe the simple hysteresis current-control strategy [9, 11] to track the reference currents. Fig. 3.6 shows the single-line schematic diagram of the DSTATCOM connected to the PCC. In the following discussion the source voltages are considered to be balanced sinusoids and the feeder impedances for all three phases are the same and equal to $R_s + j\omega L_s$. The capacitor C_f is the filter capacitor that provides a path for the high frequency switching harmonic components in the current i_d and prevents them from entering the system. In the present discussion a DC battery is used instead of the DC storage capacitor.

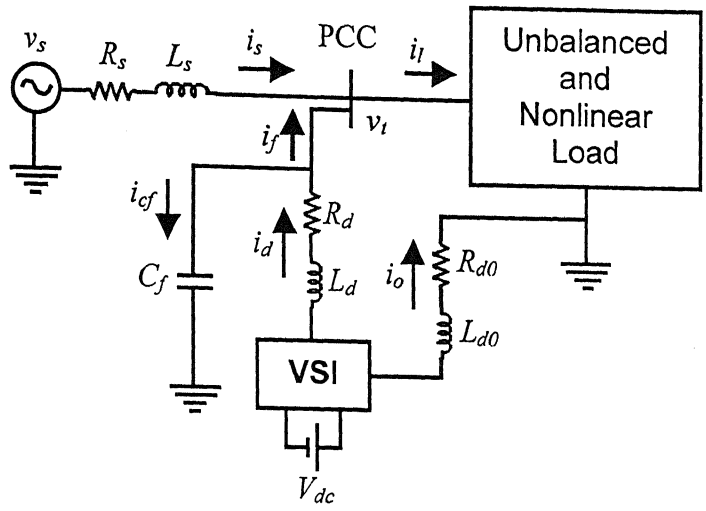

Fig. 3.6 Single-phase circuit of a DSTATCOM using LC filter

The reference currents obtained using Eqn (3.31), are the references for the current injected at the PCC (i_f). However the inverter must be made to track a reference for the current i_d. The relation between i_f and i_d can be obtained by applying KCL at the node where the filter capacitor is connected.

$$i_d = i_f + i_{cf} \tag{3.32}$$

Using Fourier online extraction the fundamental components of the terminal voltages at the PCC can be obtained using Eqn. (3.20) in Section 3.4. As the source voltages are balanced and the feeder impedances are equal in all phases the fundamental components of the terminal voltages will also be balanced sinusoids without any ripple that may remain in the terminal voltage despite the action of the filter capacitor. The references for the filter capacitor current can be obtained by

$$i_{cf}^* = C_f \frac{d}{dt}\left(v_{tf}\right) \tag{3.33}$$

The derivative is calculated by taking the ratio of two successive voltage samples with respect to the simulation time step. The above expression can be substituted in Eqn (3.32) to get the reference for the i_{da}, i_{db} and i_{dc}.

With reference to Fig. 2.10 in Chapter 2 and the subsequent discussion, the reference for the compensator current in the fourth leg is given by Eqn. (2.11) that is rewritten below

$$i_o^* = -\left(i_{la} + i_{lb} + i_{lc}\right) \tag{3.34}$$

Simulation Results

The system parameters chosen for the simulation is an extension of the system parameters given in Table 3.1. The additional parameters have been specified in Table 3.2. To prove that the algorithm can arbitrarily set the power factor, it has been desired the source current should lag the PCC voltage by 30°. Fig 3.7 shows the results of the simulation.

Table 3.2 System Parameters

System Parameters	Values of Parameters
Source Impedance	$R_s+jX_s=0.5+j3.141$ ohm
Compensator	$R_0=R_f=0.01$ ohm $L_0=L_f=40$ mH $C_f=100$ μF $V_{dc}=25$ kV $h=0.1$ A

From Fig 3.7 (a) and (c) it is observed that both the terminal voltages and source currents are balanced sinusoids despite the load currents being distorted and unbalanced as shown in Fig. 3.7 (b). Fig 3.7 (d) shows the phase a source current and terminal voltage with the latter being scaled down by a factor of 15. The source current can be seen to be lagging the PCC voltage by approximately 30°. Fig. 3.7 (e) shows the instantaneous reactive powers from which it can be observed that the compensator is not supplying the entire reactive power requirement of the load due to which the terminal reactive power has a non-zero value. This is because the PCC power factor has not been set to unity. However from Fig. 3.7 (f), the compensator is observed to supply the entire oscillating component of the instantaneous load real power. Note that the instantaneous source real power will exceed the instantaneous terminal real power by the losses in the feeder resistance.

Even though the source current and terminal voltage waveforms are seen to be smooth sinusoids due to the action of the filter capacitor, the switching frequency of the inverter is found on measurement to be approximately 12 kHz. This makes the practical implementation of the hysteresis current-control strategy difficult because of the high switching losses in the inverter.

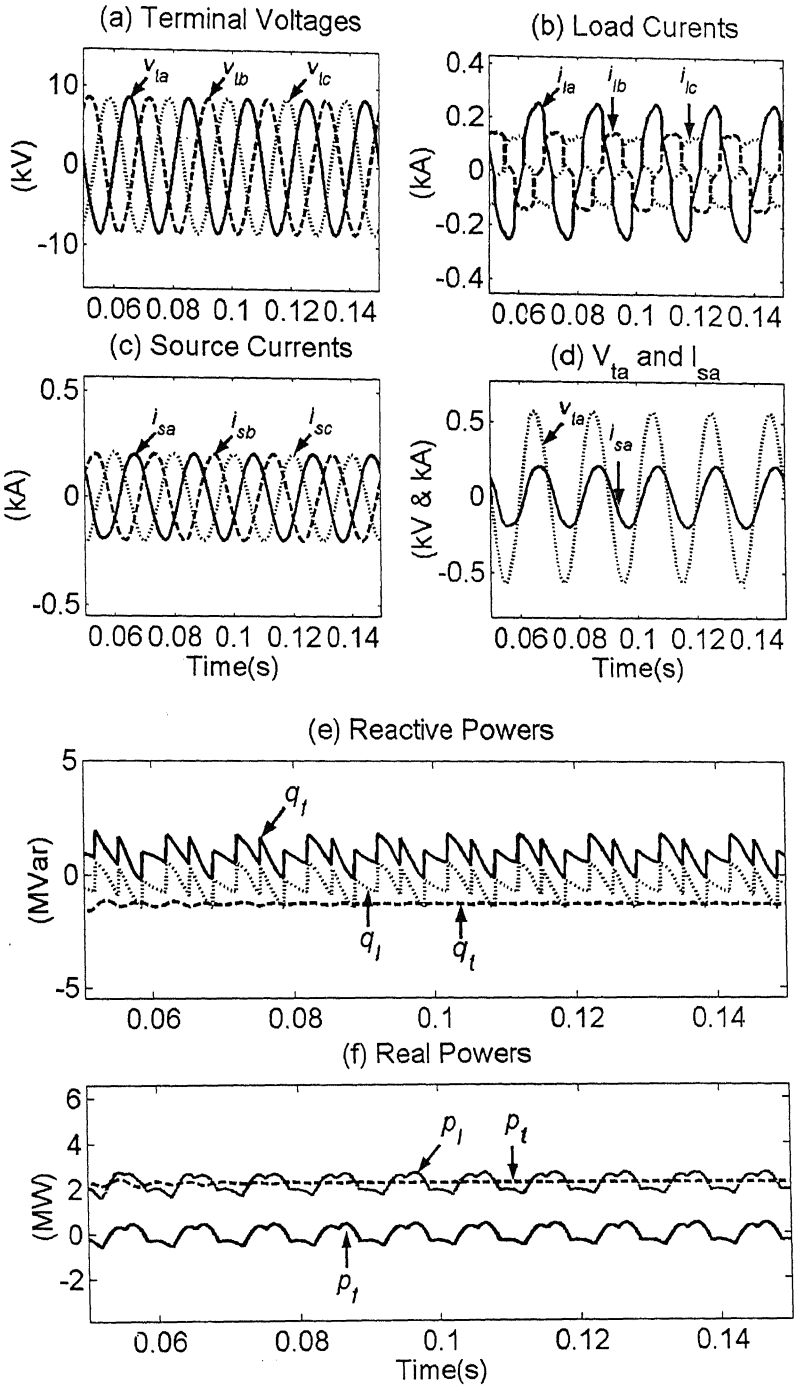

Fig. 3.7 System response with a DSTATCOM using hysteresis current control method

3.5.2 DSTATCOM Using a Pole Shift Controller

Fig 3.8 shows the single-line diagram of the DSTATCOM connected to a system with a non-stiff source. In this case a different filter structure than used in Fig. 3.6 is used. Comparing these two figures it can be seen that an inductor L_f is added before the PCC. Moreover for the neutral path capacitor C_{f0} and inductor L_{f0} are added to suppress high frequency harmonic component.

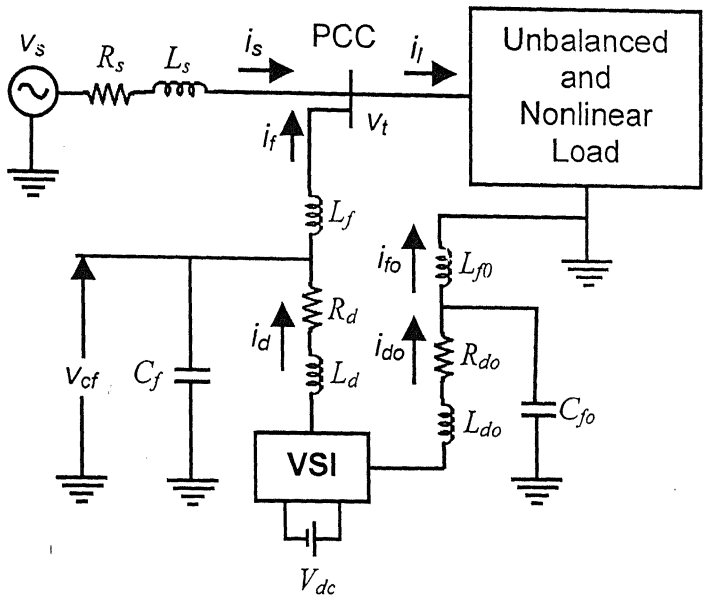

Fig. 3.8 Single-phase circuit of a DSTATCOM using LCL filter

It has been shown that hysteresis tracking for higher order systems often result in unstable feedback systems [9]. Therefore, the inverter of Fig. 3.8 cannot be controlled by a hysteresis controller. Instead, a pole shift controller will be used. In order to derive the state space equations for the shunt compensator, an equivalent circuit of the compensator connected to the PCC is drawn in Fig. 3.9. The state vector $\boldsymbol{x}$ is chosen as

$$\boldsymbol{x} = \begin{bmatrix} i_f \\ i_d \\ v_{cf} \end{bmatrix}$$

Applying KVL and KCL to the equivalent circuit in Fig. 3.9, the following state space equation is obtained

$$\begin{bmatrix} \dot{i}_f \\ \dot{i}_d \\ \dot{v}_{cf} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1/L_f \\ 0 & -R_d/L_d & -1/L_d \\ -1/C_f & 1/C_f & 0 \end{bmatrix} \begin{bmatrix} i_f \\ i_d \\ v_{cf} \end{bmatrix} + \begin{bmatrix} 0 \\ \dfrac{V_{dc}}{L_d} \\ 0 \end{bmatrix} u_c + \begin{bmatrix} -1/L_f \\ 0 \\ 0 \end{bmatrix} v_t \qquad (3.35)$$

$$\dot{\boldsymbol{x}} = \mathbf{A}\boldsymbol{x} + \mathbf{B}_u u_c + \mathbf{B}_w v_t \qquad (3.36)$$

where

$$\mathbf{A}=\begin{bmatrix} 0 & 0 & 1/L_f \\ 0 & -R_d/L_d & -1/L_d \\ -1/C_f & 1/C_f & 0 \end{bmatrix},\quad \mathbf{B}_u=\begin{bmatrix} 0 \\ \dfrac{V_{dc}}{L_d} \\ 0 \end{bmatrix},\quad \mathbf{B}_w=\begin{bmatrix} -1/L_f \\ 0 \\ 0 \end{bmatrix}$$

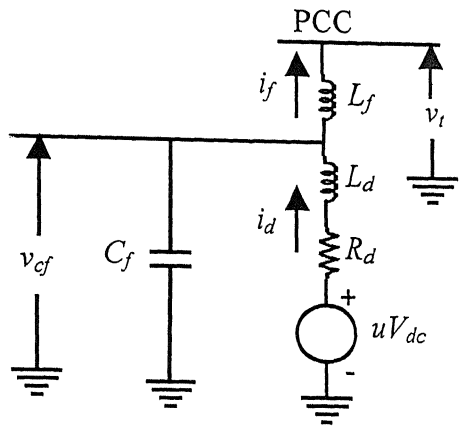

Fig. 3.9 Equivalent circuit of a DSTATCOM using LCL filter

where u_c is a smooth control action that determines the switching control $u = \pm 1$. The output is the current injected into the system (i_f). Therefore

$$y = i_f = \mathbf{C}\boldsymbol{x} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}\boldsymbol{x} \tag{3.37}$$

To implement a controller based on the above state space equation either in simulation or in practice through a digital computer or DSP processor, the state space equations will be converted to discrete form where the new state space equation will be written as

$$\boldsymbol{x}(k+1) = \mathbf{F}\boldsymbol{x}(k) + \mathbf{G}u_c(k) \tag{3.38}$$

$$y(k) = \mathbf{H}\boldsymbol{x}(k) \tag{3.39}$$

The transfer function between u_c and y of the above system in inverse z domain can be written as a ratio of two polynomials

$$G(z^{-1}) = \frac{N(z^{-1})}{D(z^{-1})} = \frac{n_1 z^{-1} + n_2 z^{-2} + n_3 z^{-3}}{1 + d_1 z^{-1} + d_2 z^{-2} + d_3 z^{-3}} \tag{3.40}$$

The characteristic equation of the above transfer function will be

$$1 + d_1 z^{-1} + d_2 z^{-2} + d_3 z^{-3} = 0 \tag{3.41}$$

The poles of the above equation will be the open-loop poles of the system. The objective is to design a feedback system as in Fig. 3.10.

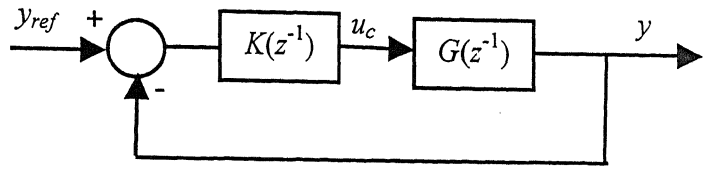

Fig. 3.10 Block diagram depicting feedback control

Let the transfer function of the controller be given as

$$K(z^{-1}) = \frac{S(z^{-1})}{R(z^{-1})} = \frac{s_0 + s_1 z^{-1} + s_2 z^{-2}}{1 + r_1 z^{-1} + r_2 z^{-2}} \tag{3.42}$$

Then the characteristic equation of the closed loop system is

$$1 + \frac{N(z^{-1})S(z^{-1})}{D(z^{-1})R(z^{-1})} = 0$$

$$i.e., D(z^{-1})R(z^{-1}) + N(z^{-1})S(z^{-1}) = 0 \tag{3.43}$$

For a pole shift control, to obtain the closed loop poles the open loop poles are shifted by a factor λ. The factor λ is called the pole shift factor and is constrained by $0 < \lambda < 1$. Hence the closed loop characteristic equation can be written as a modification of the open loop characteristic equation as follows [9, 10]

$$1 + \lambda d_1 z^{-1} + \lambda^2 d_2 z^{-2} + \lambda^3 d_3 z^{-3} = 0 \tag{3.44}$$

Solving the Eqns (3.43) and (3.44), the feedback transfer function $K(z^{-1})$ can be determined. Hence at any given instant the difference between the reference for the output (i_f^*) and the output (i_f) will produce a control signal u_c. This signal u_c can be used to control the switching of the VSI by subjecting it to hysteresis control to generate the switching control input as follows

If $u_c > h$ then $u = 1$

$u_c < -h$ then $u = -1$

The pole shift factor λ is the penalty imposed upon the control. For values of λ close to unity the control action will be small and hence the probability of instability will be small.

Simulation Results:

The system parameters as far as the source, load and feeder impedances are considered are the same as those in Table 3.1 and 3.2. The compensator parameters are as follows

$$L_d = 20 \text{ mH}, L_{d0} = 20 \text{ mH}$$
$$R_d = 0.01 \text{ ohm}, R_{d0} = 0.01 \text{ ohm}$$
$$L_f = 100 \text{ μH}, L_{f0} = 500 \text{ μH}$$
$$C_f = 2 \text{ μF}, C_{f0} = 15 \text{ μF}$$
$$V_{dc} = 25 \text{ kV}$$

The amount of ripple in the neutral current is larger than that in the phase current. This is because the neutral current is the sum of all the load currents. Therefore, to bypass high frequency harmonics in the neutral current, a larger filter capacitor (C_{f0}) is chosen compared to that of C_f. It is to be noted that four independent pole shift controllers are required – one for each of the three phases and one for the neutral. Out of these four, controllers for individual phases are identical but the parameters of the neutral controller are different. The pole shift factor of 0.8 is chosen for all the controllers. The feedback transfer function is calculated by solving Eqn (3.43) and (3.44) in MATLAB. For the three phases they are found to be

$$\frac{S(z^{-1})}{R(z^{-1})} = \frac{10.6942 - 19.5244z^{-1} + 8.9703z^{-3}}{1 + 0.4796z^{-1} + 0.0996z^{-2}}$$

The feedback transfer function for the neutral leg is

$$\frac{S(z^{-1})}{R(z^{-1})} = \frac{17.1876 - 31.3426z^{-1} + 14.3612z^{-3}}{1 + 0.4799z^{-1} + 0.0997z^{-2}}$$

The control input signal u_c that is generated by the feedback path is applied to a hysteresis control as described before to generate the switching control input u.

In the simulation the PCC is required to be at unity power factor. Fig. (3.11) shows the results of the simulation. From Fig. 3.11 (a) and (c) it is observed that the terminal voltages and the source currents are balanced sinusoids for a load that draws a distorted and unbalanced current. Fig. 3.11 (d) shows that the source currents are in phase with the terminal voltages and hence the PCC is at unity power factor. Fig. 3.11 (e) shows that the compensator supplies the entire instantaneous load reactive power. Fig. 3.11 (f) shows that the compensator supplies the oscillating component of the

instantaneous load real power. The switching frequency of the VSI was observed to be 7kHz. This is an appreciable improvement over the hysteresis current-control strategy discussed in Section 3.6.1. Hence the switching losses have been reduced to a large extent.

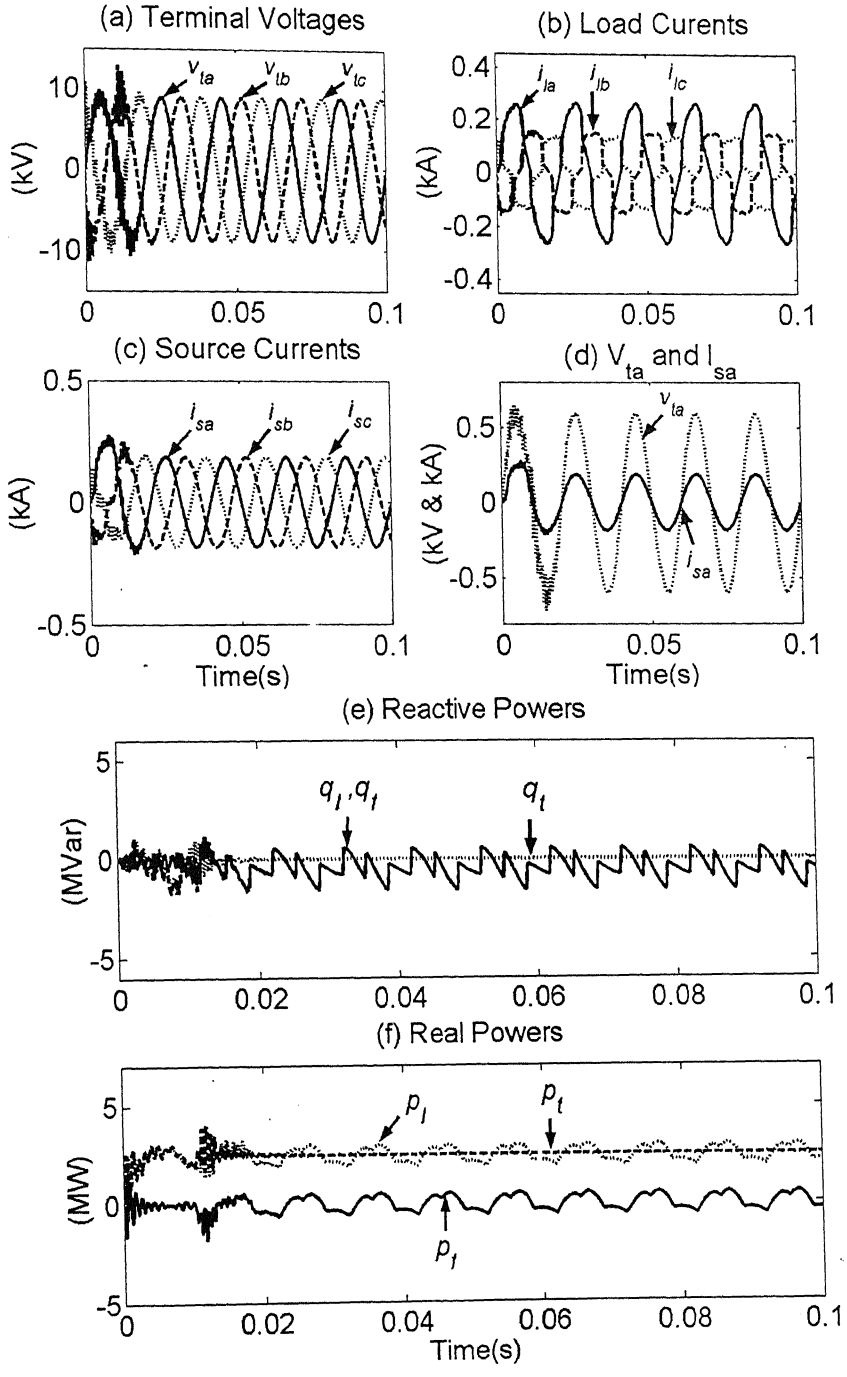

Fig. 3.11 System response for a DSTATCOM using pole shift controller

3.5.3 DSTATCOM Using State Feedback Control

The single-phase circuit for a DSTATCOM controlled using the state feedback control strategy [9, 10, 15] is the same as that given in Fig 3.6. The equivalent circuit required for writing the state space equations is given below in Fig. 3.12.

In the above figure load is represented as a simple RL load without any attempt to model non-linearity.

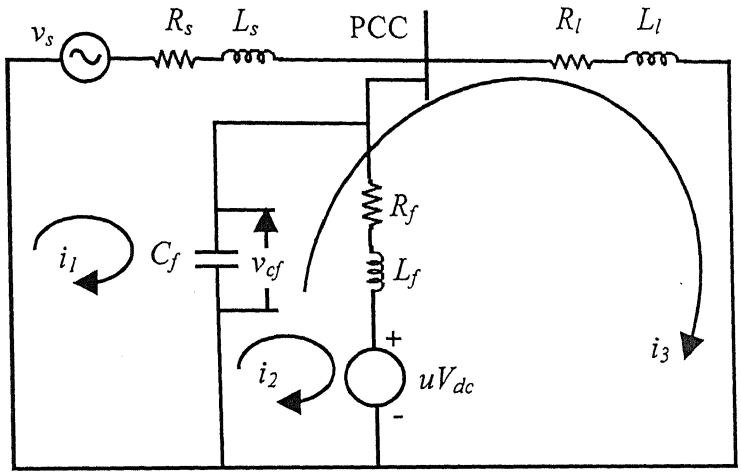

Fig. 3.12 Equivalent circuit of a system having a DSTATCOM with LC filter

The state vector is assumed to be

$$x = \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_{cf} \end{bmatrix}$$

Applying KVL and KCL to the equivalent circuit in Fig 3.12 the following state space equation is obtained

$$\dot{x} = \begin{bmatrix} -\frac{R_s}{L_s} & 0 & 0 & -\frac{1}{L_s} \\ 0 & -\frac{R_f}{L_f} & 0 & \frac{1}{L_f} \\ 0 & 0 & -\frac{R_l}{L_l} & \frac{1}{L_l} \\ \frac{1}{C_f} & -\frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} x + \begin{bmatrix} 0 \\ -\frac{V_{dc}}{L_f} \\ 0 \\ 0 \end{bmatrix} u_c + \begin{bmatrix} \frac{1}{L_s} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_s \qquad (3.45)$$

$$\dot{x} = \mathbf{A}x + \mathbf{B}_u u_c + \mathbf{B}_w v_s \qquad (3.46)$$

For convenience of reference generation a state transformation is performed to change the state variable as follows

$$z = \begin{bmatrix} i_f \\ i_{cf} \\ v_t \\ i_l \end{bmatrix} = \begin{bmatrix} -1 & 0 & 1 & 0 \\ 1 & -1 & -1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} x = Px \tag{3.47}$$

The state space equation is then transformed into

$$\dot{z} = PAP^{-1}z + P\mathbf{B}_u u_c + P\mathbf{B}_w v_s \tag{3.48}$$

The next objective is to design a feedback matrix such that

$$u_c = -K(z - z_{ref}) \tag{3.49}$$

The control signal obtained can be used to control the switching of the VSI by applying it to a hysteresis control to obtain the switching control input u.

Simulation Results:

The system parameters are the same as in Table 3.1 and the feeder impedance is the same as in Table 3.2. The specifications of the compensator are as follows

$$L_d = L_{d0} = 40 \text{ mH}$$
$$R_d = R_{d0} = 0.01 \text{ ohm}$$
$$C_f = 50 \ \mu\text{F}$$
$$V_{dc} = 25 \text{ kV}$$

A Linear Quadratic Regulator (LQR) control [9] is employed to design the feedback gain matrix K. The following state weighting matrix Q and control weighting r are chosen

$$Q = \begin{bmatrix} 18 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}, \quad r = 1$$

The state weighting matrix Q reflects the importance of the states. The feedback gain matrix K' is found using the Control Systems Toolbox in MATLAB to give the state feedback matrix as follows

$$K' = [3.8834 \quad 1.0324 \quad 1.0281 \quad -2.1789]$$

With the above feedback matrix, the eigenvalues of the closed loop system are to the left of the straight line s = -354.79. Since the load is unpredictable and liable to change, a reference for the load current is difficult to set. Hence the last element of the matrix K' is set to zero. Hence the feedback matrix becomes

$$K = [3.8834 \quad 1.0324 \quad 1.0281 \quad 0]$$

This causes a change in the eigenvalues of the closed loop system which are now left of the straight line s = -297.97. This minimal shift in the eigenvalues will not affect the stability of the closed loop system. A further demonstration of the robustness of the controller for changes in the system parameters can be presented in Table 3.3 where all the entries are the maximum eigenvalues of the closed loop system.

Table 3.3

System Parameters	20% Decrease	10% Decrease	Nominal Values	10% Increase	20% Increase
Feeder Impedances	-351.67	-322.29	-297.97	-277.55	-260.18

In the simulation, the PCC is required to be at unity power factor. Fig. 3.13 shows the simulation results. The results are very similar to the Section 3.6.2 shown in Fig. 3.11. The switching frequency of the VSI is 4.5 kHz that is a further improvement over the pole shift controller.

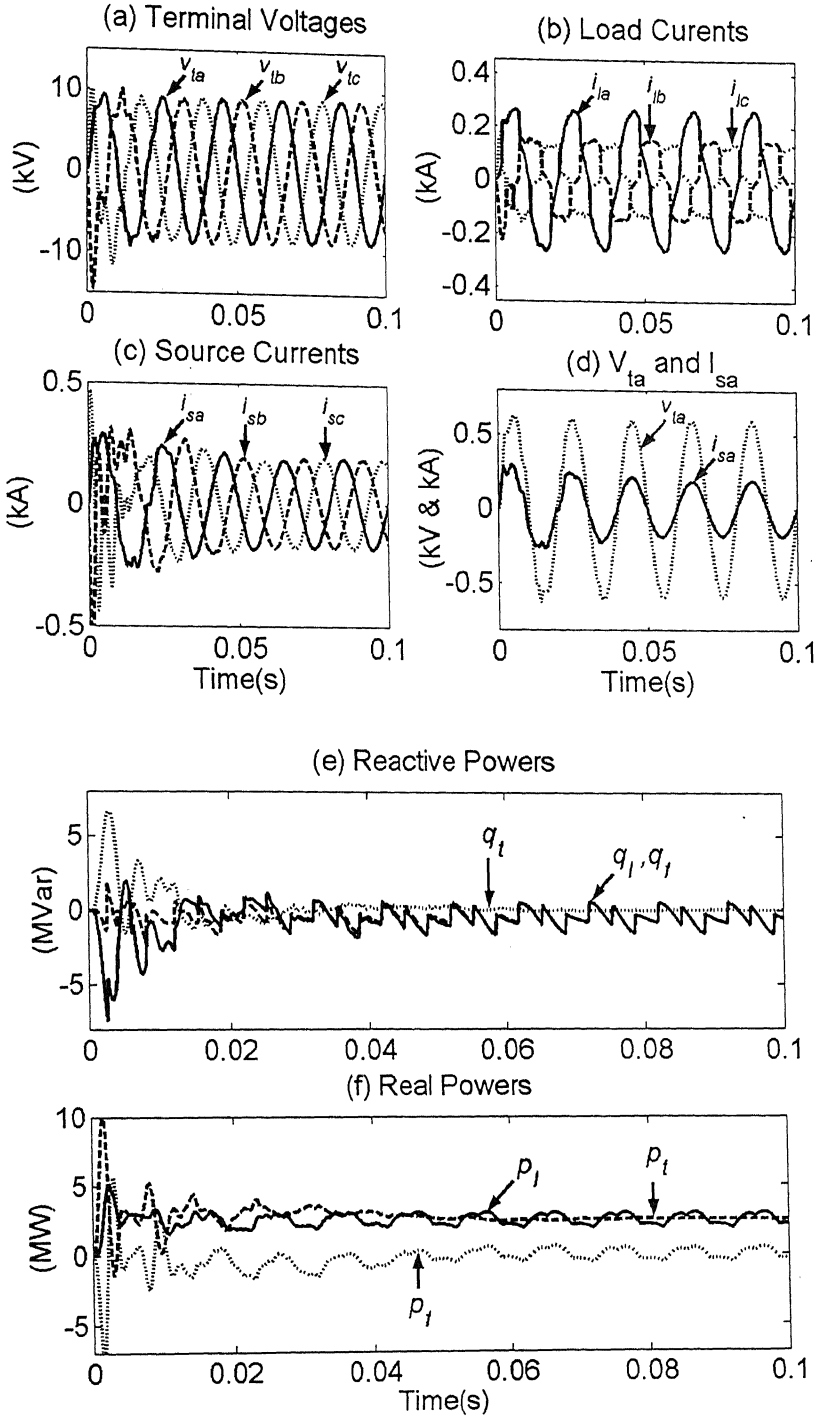

Fig. 3.13 System response with a DSTATCOM using state feedback controller

3.6 CONTROL OF DC STORAGE CAPACITOR VOLTAGE

In the previous sections the energy storage element in the inverter was considered to be a DC battery. If the DC battery were to be replaced by a DC storage

capacitor, the algorithm will have to be modified [9]. The capacitor voltage can be maintained despite the losses in the inverter circuit by drawing an amount of power from the ac system.

Therefore, the voltage drop of the capacitor from its nominal value can be used in a proportional plus integral (PI) controller as follows

$$v_e = v_{cref} - v_c$$

$$p_{loss} = K_p v_e + K_I \int (v_e) dt \tag{3.50}$$

where p_{loss} signifies the power loss in the inverter circuit. Since this power must also come from the PCC, Eqn (3.29) in Section 3.5 is modified to

$$V_{ta1f} I_{sa1} \cos(\phi) = p_{lav} + p_{loss} \tag{3.51}$$

The corresponding references for the compensator currents are then found using Eqn (3.31).

Simulation Results:

In the compensator used in Section 3.6.4 a DC storage capacitor of 10000 μF is used and is considered to be pre-charged to 25 kV. The parameters of the PI controller chosen by trial and error are

$$K_p = 5,\ K_I = 13.33$$

The source voltages and feeder impedance are identical to the previous simulation. In order to study the performance of the PI controller in controlling the voltage of the DC storage capacitor, the load impedance are initially taken to be very high without any non-linearity and at 0.5 seconds the load impedances are changed to the values chosen in the previous simulation. The initial values of load impedances are

$$Z_a = 250 + j3.1416 \text{ ohm},\ Z_b = 850 + j12.565 \text{ ohm},\ Z_c = 1110 + j22.0 \text{ ohm}$$

Fig 3.14 shows the simulation results. As can be observed from Fig. 3.14 (a) and (b), the abrupt change in load impedances causes a similar change in source currents and instantaneous powers. The system reaches its new steady state after approximately 8 cycles. Fig. 3.14 (c) shows the voltage of the DC storage capacitor. When the load power demand increases suddenly at 0.5 seconds, the capacitor momentarily supplies the additional load real power and this causes the voltage to dip.

Due to the action of the PI controller, the voltage returns back to the reference value of 25 kV.

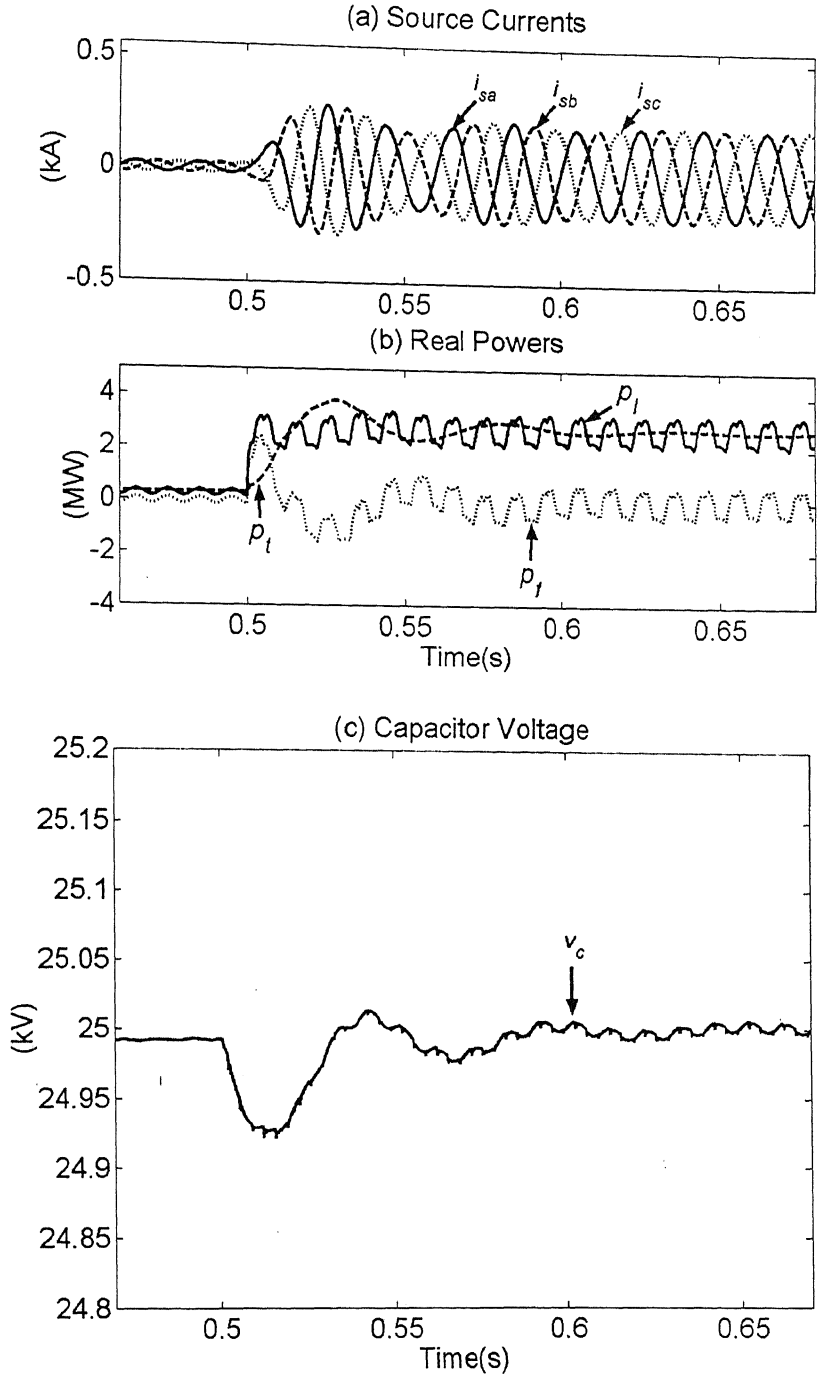

Fig. 3.14 System response for a DSTATCOM with DC storage capacitor in the case of increase in load.

An opposite response will be observed in the case of a sudden decrease in load current. In that case, as the real power demand of the load will decrease but the real power entering the terminal cannot change instantaneously. Hence the DSTATCOM will have to absorb the real power and the voltage of the DC storage capacitor will rise.

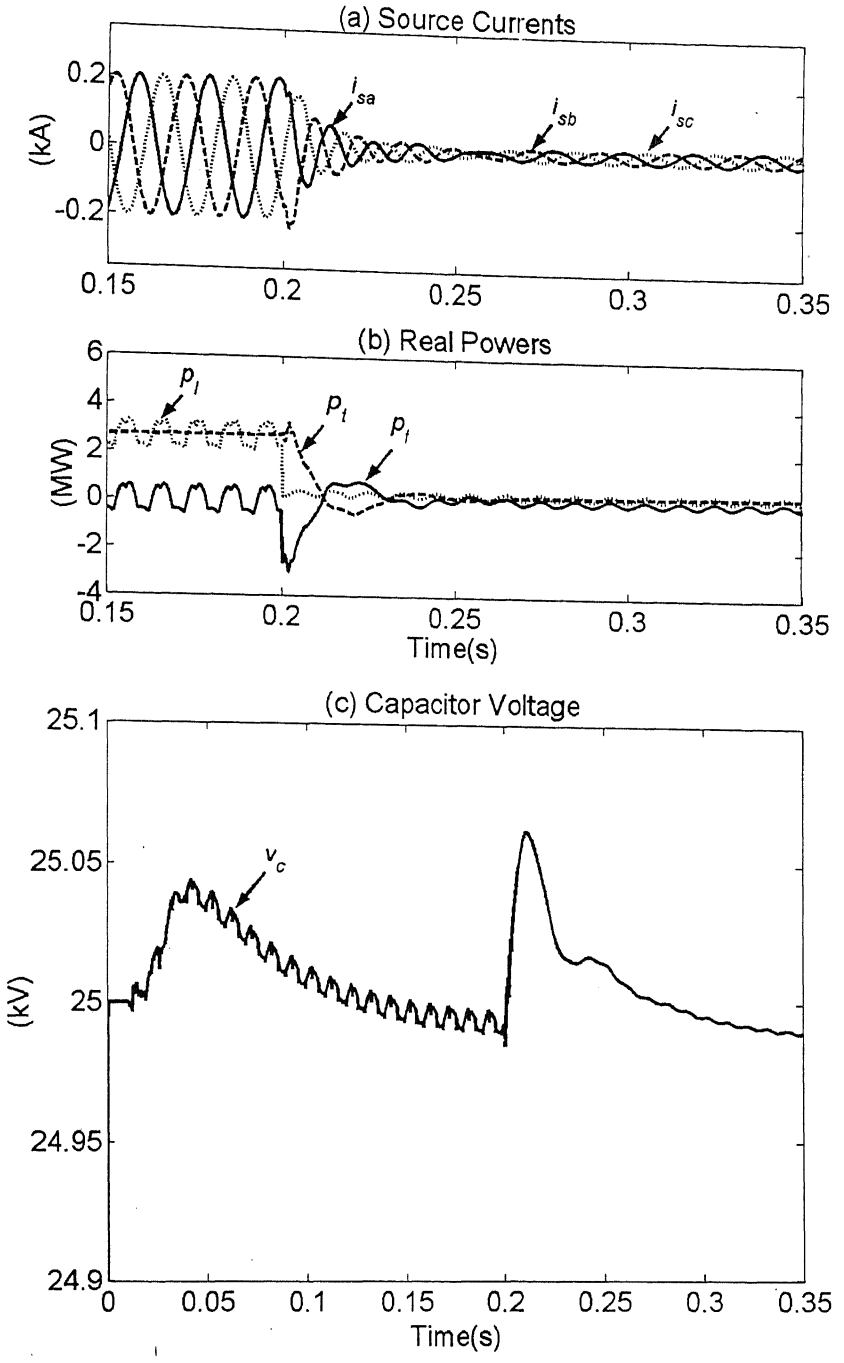

Fig. 3.15 System response for a DSTATCOM with DC storage capacitor in the case of decrease in load.

The action of the PI controller will return the voltage of the DC storage back to the reference value of 25 kV. To demonstrate this we shall assume that initially the load parameters to be equal to those in Table 3.1. After a time period of 0.2 s the load is decreased such that the load impedances become

$$Z_a = 250 + j3.1416 \text{ ohm}, Z_b = 850 + j12.565 \text{ ohm}, Z_c = 1110 + j22.0 \text{ ohm}$$

Fig. 3.14 shows the simulation results that support the explanation provided above.

3.7 DSTATCOM CONNECTED TO A SYSTEM WITH DC CURRENT

In the previous sections, the load was considered to be drawing a current that was symmetrical and hence the load current contained no DC component. However, if the load were to contain a half-wave rectifier, the load current would have a DC component. In this section, in addition to the passive load and three-phase diode rectifier, a single-phase half-wave diode rectifier is connected between phase C and the neutral. Hence the load current of phase C will have an offset. The output of the half-wave diode rectifier is connected to an RL load

$$R + jX = 100 + j\,12.56 \text{ ohm}$$

The parameters of the PI controller are the same as in the previous section

Due to the DC component in the current the instantaneous load power will contain a fundamental frequency component in addition to the other oscillating components. To filter this fundamental frequency component while obtaining p_{lav}, the instantaneous load power is averaged over a period of one cycle instead of half a cycle. This would imply a greater delay in the source currents becoming balanced sinusoids.

Fig 3.15 shows the simulation results. The load currents are unbalanced and distorted but the phase C load current has a DC shift. The source currents are balanced sinusoids. Fig. 3.15 (e) shows the voltage of the DC storage capacitor. Even though the capacitor is pre-charged to 25 kV, the PI controller of the DC loop is switched on at 10 ms. This causes the transient in the dc voltage.

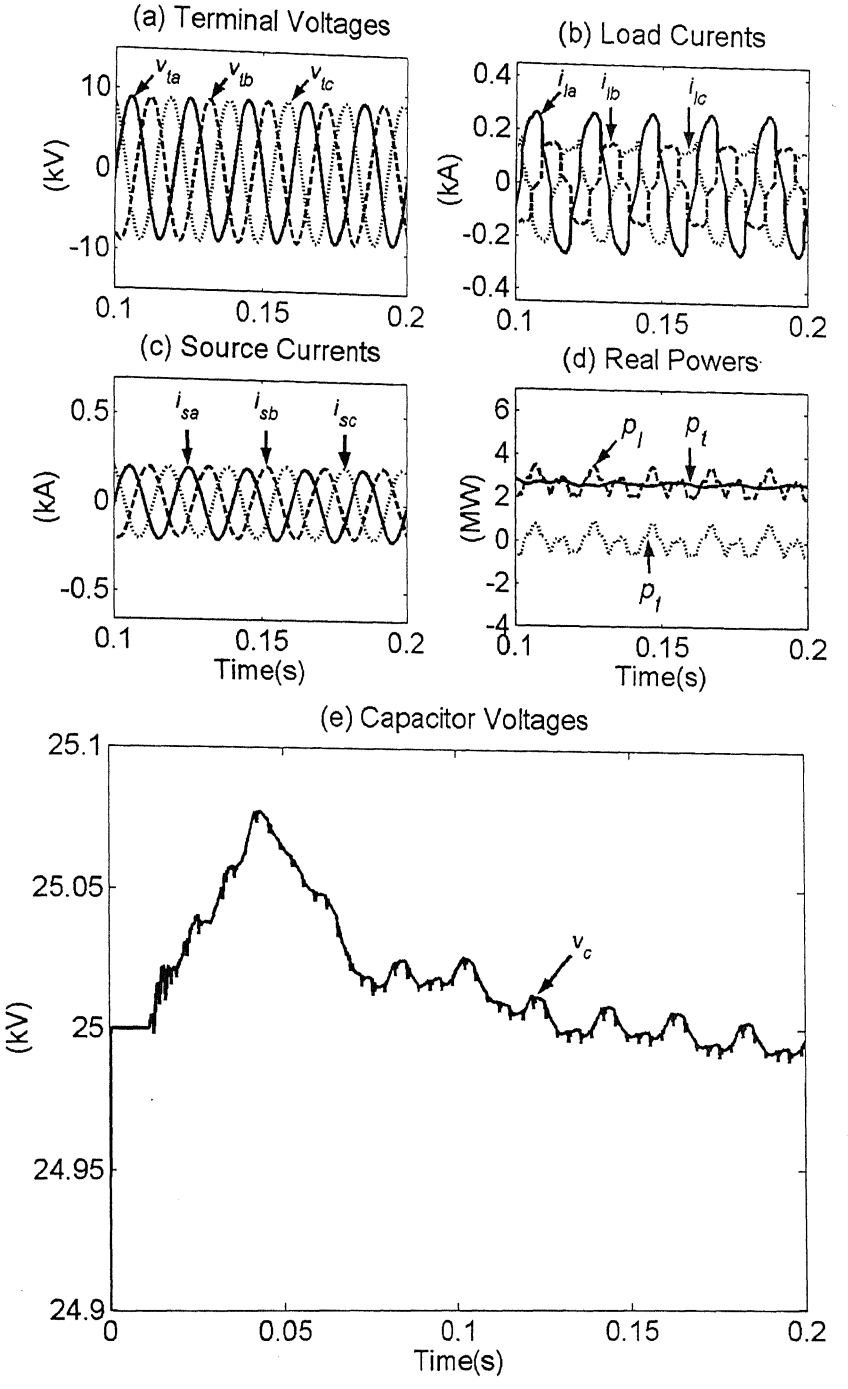

Fig. 3.16 System response with a DSTACOM in the case of load currents having an offset.

3.8 DSTATCOM CONNECTED TO AN UNBALANCED, DISTORTED AND NON-STIFF SOURCE

In the previous sections the source voltages have always been considered to be balanced sinusoids even though the algorithm used was applicable to systems where the source voltages are not balanced sinusoids. The hysteresis current-control strategy will

not be used because of the extremely high switching frequency of the VSI. In the state feedback control strategy described in Section 3.6.4, references are required not only for the current actually injected by the compensator into the PCC but also for the terminal voltages and the current through the filter capacitor. If the source were considered to be non-stiff and the source voltages have unpredictable and large number of harmonics, setting a reference for the terminal voltages will be difficult. In the pole shift control strategy described in Section 3.6.3, the only reference required is that of the current injected at the PCC. Hence for the purpose of compensating systems having unbalance and distortion in the source in addition to the load current, the pole shift strategy is more well-suited and is used here.

The system parameters as far as the load, feeder impedance and compensator parameters are concerned are the same as the simulation in Section 3.6.2. The parameters of the PI controller for controlling the DC storage capacitor voltage are the same as before.

The source voltages are unbalanced and contain 5^{th} and 7^{th} harmonics. They are given in kV are as

$$v_{sa} = 9.0\sin(100\pi t) + 1.0\sin(5*(100\pi t)) + 0.5\sin(7*(100\pi t))$$
$$v_{sb} = 7.56\sin(100\pi t - 2\pi/3) + 1.0\sin(5*(100\pi t - 2\pi/3)) + 0.5\sin(7*(100\pi t - 2\pi/3))$$
$$v_{sc} = 10.4\sin(100\pi t + 2\pi/3) + 1.0\sin(7*(100\pi t + 2\pi/3)) + 0.5\sin(7*(100\pi t + 2\pi/3))$$

Fig. 3.15 shows the simulation results. Fig. 3.15(a) and (b) shows the terminal voltages and load currents to be unbalanced and distorted. However Fig. 3.15 (c) shows the source currents to be balanced sinusoids. From Fig. 3.15 (d), which shows the instantaneous real powers, the source power is not because the source voltages are unbalanced and distorted. However, the DSTATCOM is drawing a real power with a zero mean. Fig. 3.15 (e) shows the DC storage capacitor voltage that is maintained at approximately 25 kV due to the action of the PI controller.

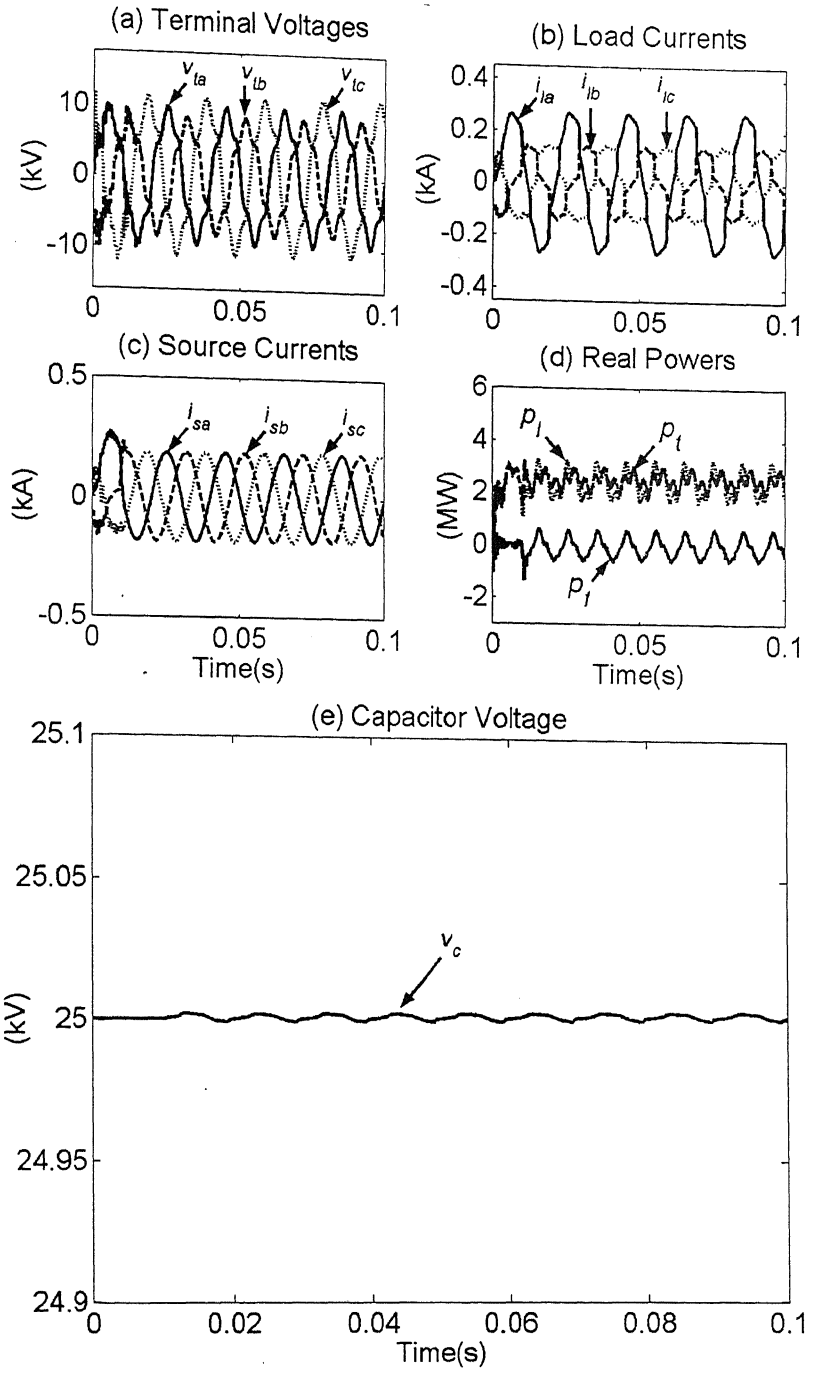

Fig. 3.17 System response with DSTATCOM for unbalanced and distorted source voltages

3.9 CONCLUSIONS

In this chapter, an algorithm has been developed for generating references for the compensator current in a three-phase four-wire distribution system with unbalanced and distorted non-stiff source and unbalanced and non-linear load such that the source currents is balanced and sinusoidal. Two different filter structures have been used to

bypass the high frequency harmonic components generated by the switching of the VSI. Three control strategies, namely the hysteresis controller, pole shift controller and state feedback controller have been implemented to control the switching of the VSI so that the actual currents track the references as closely as possible. The application of the hysteresis controller is limited due to the high switching frequency of the VSI. The state feedback control strategy applied to the DSTATCOM with a capacitor filter across the PCC shown in Fig. 3.6 would be most preferred in the case when the source voltages are balanced sinusoids as the switching frequency of the VSI is the lowest at 4.5 kHz. However, when the source voltages may not be balanced sinusoids, the pole shift control strategy for the DSTATCOM having the filter structure shown in Fig. 3.8 will be used. The use of the four-leg inverter for compensating systems with unbalanced and non-linear load, unbalanced and distorted source voltages and for loads drawing a DC component has been proved.

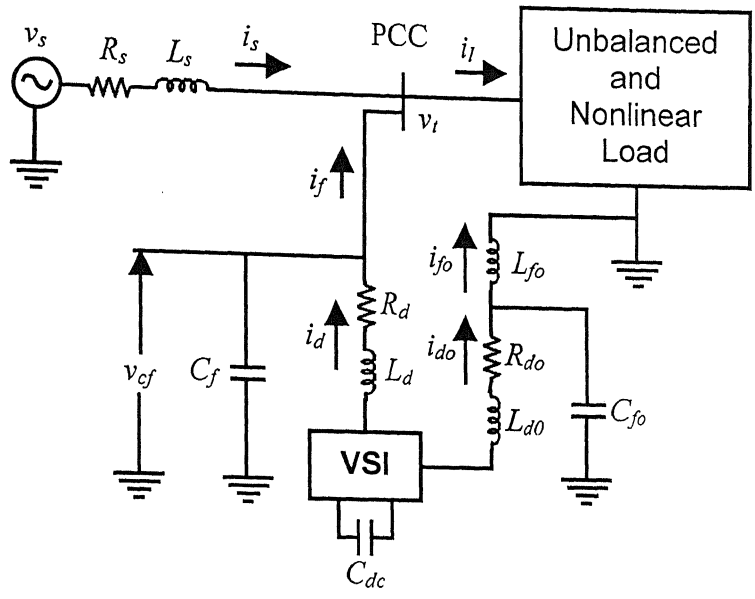

Fig. 4.1 Single-phase diagram of a DSTATCOM in voltage-controlled mode using four-leg VSI

The references for the PCC voltages will have a peak of 9 kV but the phase angle will be such that the DSTATCOM neither absorbs nor supplies any average real power in the steady state. The best indication of whether the compensator is involved in any transfer of average real power is the deviation of the DC storage capacitor voltage from its reference value. If the compensator were supplying average real power, the DC capacitor voltage will fall from its reference value, whereas if it were absorbing average real power its voltage would increase. Hence the phase angle of the reference for the phase a PCC voltage can be set as follows [9, 19]

$$\phi_{ta}^{*} = -K_p\left(v_{cref} - v_c\right) - K_I \int\left(v_{cref} - v_c\right)dt \tag{4.1}$$

The phase angle references for phase b and c will be

$$\phi_{tb}^{*} = \phi_{ta}^{*} - 120°$$

$$\phi_{tc}^{*} = \phi_{ta}^{*} - 240°$$

where K_p and K_I are the parameters of the proportional-integral (PI) controller. Hence, feeding the error between the reference capacitor voltage and the actual capacitor voltage to the PI controller sets the phase angle for the reference PCC voltage. Hence,

$$v_{tk}^{*} = 9.0\sin\left(100\pi t + \phi_{tk}^{*}\right) \tag{4.2}$$

where $k = a, b, c$

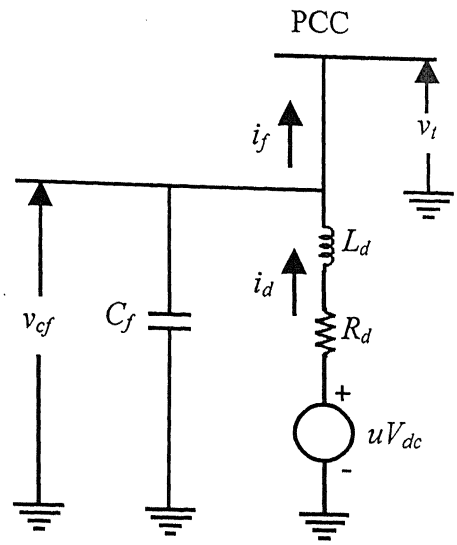

Fig. 4.2 Equivalent circuit of the DSTATCOM

The single-phase equivalent circuit of the single-phase circuit of the DSTATCOM is shown in Fig. 4.2.

The state space vector for the above equivalent circuit is chosen as

$$\boldsymbol{x} = \begin{bmatrix} v_t \\ i_d \end{bmatrix}$$

The state space equation can be written as

$$\dot{\boldsymbol{x}} = \begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{L_d} & -\frac{R_d}{L_d} \end{bmatrix} \boldsymbol{x} + \begin{bmatrix} 0 \\ -V_{dc}/L_d \end{bmatrix} u_c + \begin{bmatrix} -1/C_f \\ 0 \end{bmatrix} i_f \tag{4.3}$$

$$\dot{\boldsymbol{x}} = \mathbf{A}\boldsymbol{x} + \mathbf{B}_u u_c + \mathbf{B}_w i_f \tag{4.4}$$

The output variable is the PCC voltage v_t which is the variable that is required to regulated. Hence

$$y = v_t = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} v_t \\ i_d \end{bmatrix} \tag{4.5}$$

$$y = \mathbf{C}\boldsymbol{x} \tag{4.6}$$

The aim is to make the PCC voltages track the respective references. However, it would not be possible to set a reference for the inverter current i_d. Due to this, instead

of using a full state feedback control where a reference for i_d would be required, a pole shift controller [9, 10] is used which uses only the output variable v_t.

The state space equations derived above are discretized and the transfer function between u_c and y in the inverse z domain is written as follows

$$\frac{N(z^{-1})}{D(z^{-1})} = \frac{n_1 z^{-1} + n_2 z^{-2}}{1 + d_1 z^{-1} + d_2 z^{-2}} \tag{4.7}$$

Hence the open loop poles are the roots the characteristic equation

$$1 + d_1 z^{-1} + d_2 z^{-2} = 0 \tag{4.8}$$

The transfer function of the pole shift controller is given as

$$\frac{S(z^{-1})}{R(z^{-1})} = \frac{s_0 + s_1 z^{-1}}{1 + r_1 z^{-1}} \tag{4.9}$$

The closed-loop characteristic equation is written as

$$D(z^{-1})R(z^{-1}) + N(z^{-1})S(z^{-1}) = 0 \tag{4.10}$$

By using the pole shift factor λ ($0 < \lambda < 1$) as described in Section 3.6.5, the closed-loop characteristic equation is written as

$$1 + d_1 \lambda z^{-1} + d_2 \lambda^2 z^{-2} = 0 \tag{4.11}$$

Solving equations (4.9) and (4.11), the feedback transfer function can be obtained. The control input signal is obtained by

$$u_c(k) = \frac{S(z^{-1})}{R(z^{-1})}\left(y_{ref}(k) - y(k)\right) \tag{4.12}$$

This control signal is applied to a hysteresis controller to obtain the switching control logic as follows

If $u_c > h$ then $u = 1$

$u_c < -h$ then $u = -1$

The fourth leg of the VSI works in current control mode and uses a pole shift controller in the same manner as in Section 3.6.5. The reference current for the fourth leg is given by

$$i_0^* = \left(i_{sa} + i_{sb} + i_{sc}\right) - \left(i_{la} + i_{lb} + i_{lc}\right) \tag{4.13}$$

4.2 SIMULATION RESULTS

The parameters of the system chosen for the simulation are listed in Table 4.1

Table 4.1 System Parameters

System Parameters	Values of Parameters
Source Voltages in kV	$v_{a1} = 9.0\sin(100\pi t) + 2.5\sin(5*(100\pi t)) + 1.4\sin(7*(100\pi t))$ $v_{b1} = 10.4\sin(100\pi t - 2\pi/3) + 2.5\sin(5*(100\pi t - 2\pi/3)) + 1.4\sin(7*(100\pi t - 2\pi/3))$ $v_{c1} = 7.5\sin(100\pi t + 2\pi/3) + 2.5\sin(5*(100\pi t + 2\pi/3)) + 1.4\sin(7*(100\pi t + 2\pi/3))$
Feeder Impedance	$R_s + jX_s = 0.5 + j3.141\ \Omega$
Load	Passive RL load as follows Z_a=50+j21.98 Ω Z_b=170+j31.41 Ω Zc=222+j125.64 Ω
	Three-phase Diode Rectifier having the following RL load at its output Z_L=150+j12.56 Ω
Compensator Parameters	$C_{dc} = 10000\ \mu F$ $L_d = 20$ mH, $L_{d0} = 15$ mH $R_d = 0.01\ \Omega$, $R_{d0} = 0.01\ \Omega$ $C_f = 20\ \mu F$, $C_{f0} = 15\ \mu F$ $L_{f0} = 500\ \mu H$ $v_{cref} = 30$ kV

The PI controller parameters for setting the phase angle of the reference PCC voltage are

$K_p = 10, K_I = 10$

The feedback matrix for the three legs of the VSI connected to the PCC is calculated using the Control Systems Toolbox in MATLAB which solves Eqns (4.9) and (4.11) taking pole shift factor $\lambda = 0.8$ and are found to be

$$\frac{S(z^{-1})}{R(z^{-1})} = \frac{0.081 - 0.079z^{-1}}{1 + 0.0494z^{-1}}$$

The feedback matrix for the fourth leg of the VSI connected to the neutral is

$$\frac{S(z^{-1})}{R(z^{-1})} = \frac{7.13 - 13.0z^{-1} + 5.9802z^{-2}}{1 + 0.4796z^{-1} + 0.0996z^{-2}}$$

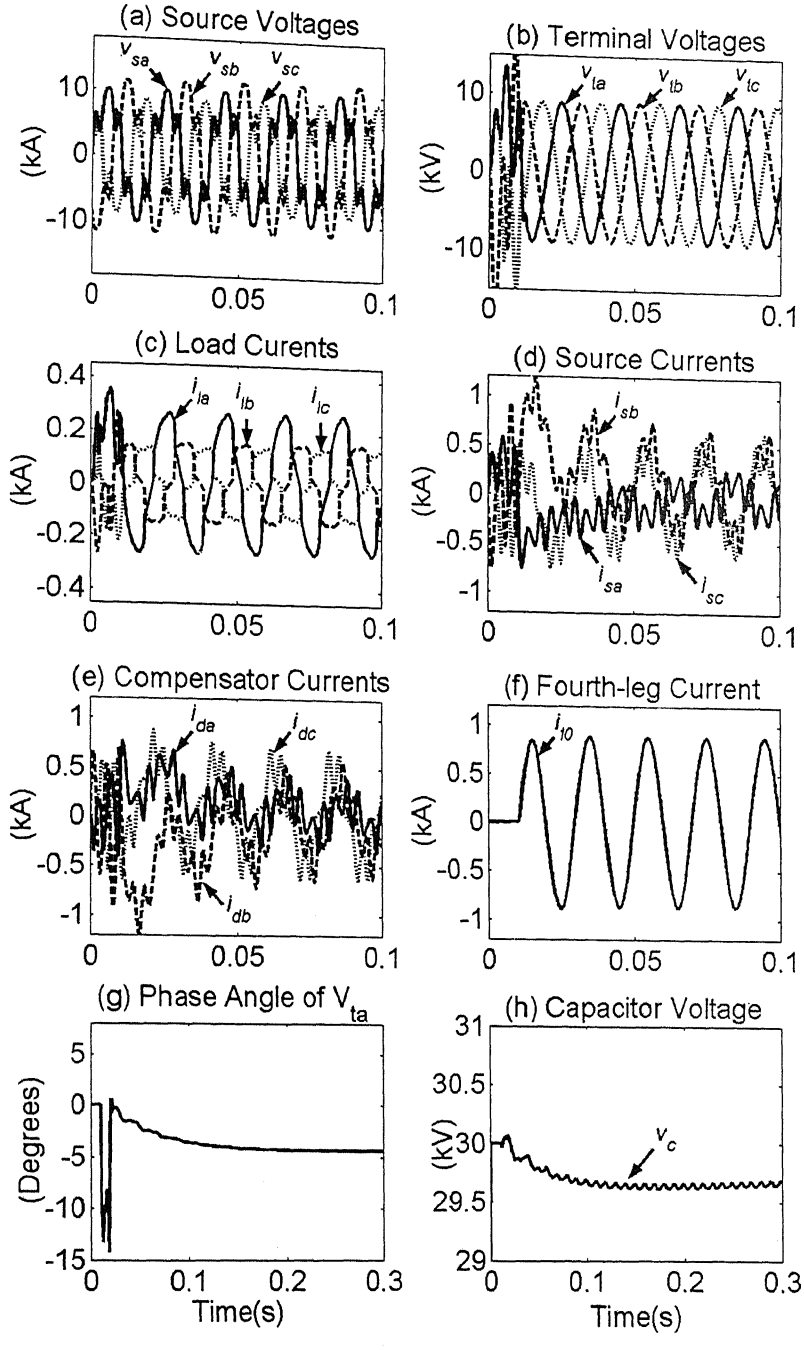

Fig. 4.3 System response with a DSTATCOM for unbalanced and distorted source voltages

Fig 4.3 shows the simulation results. Fig. 4.3 (a) shows the source voltages to be unbalanced and distorted but the terminal voltages as seen in Fig. 4.3 (b) are balanced, sinusoidal and regulated at 9 kV. Fig. 4.3 (c) shows the load currents to be unbalanced and distorted. Fig. 4.3 (d) and (e) shows the source currents and compensator currents to be unbalanced and distorted. Moreover, they are larger in magnitude than the load currents. Fig. 4.3 (f) shows the currents injected by the fourth leg of the compensator. Fig. 4.3 (g) shows the phase angle of the PCC voltage of phase a which, after initial

oscillations, settles at an angle of approximately –4.5°. Fig. 4.3 (f) shows the voltage of the DC storage capacitor that is pre-charged to 30 kV. The voltage begins returning back to its reference value after the initial dip when the compensator is turned on. The DC capacitor voltage returns back to the reference value of 30 kV after approximately 1.7 seconds. As the DC capacitor voltage does not drop below 29.5 kV, the tracking performance is not affected. The switching frequency of the VSI is approximately 8.5 kHz.

4.3 OPERATION OF DSTATCOM IN THE CASE OF CHANGE IN LOAD

In the previous section, all the system parameters were assumed to be constant throughout the simulation. In this section, the operation of the compensator is studied in the case of a sudden increase in load current. Initially the load is only an unbalanced load with no non-linearity having the following parameters

$R_a + jX_a = 250 + j21.98$ ohm

$R_b + jX_b = 850 + j31.41$ ohm

$R_c + jX_c = 1110 + j125.64$ ohm

After 0.3 seconds a load change is considered in which the load is equal to that given in Table 4.1. Due to the sudden increase in the load current, the increased real power demand of the load cannot be met instantaneously by the supply. Hence, the compensator will momentarily supply the additional real power demand. Under the circumstances, the PI controller must regulate the voltage of the DC storage capacitor by adjusting the phase angle of the reference PCC voltages. All other parameters of the system are the same as in Table 4.1. The feedback matrix and the parameters of the PI controller are the same as in the previous section.

Fig 4.4 shows the simulation results. Fig 4.4 (a) shows the source voltages to be unbalanced and distorted. They are identical to the waveforms in Fig. 4.3 (a). Fig. 4.4 (c) shows the load currents. Before 0.3 seconds, the load current is seen to be negligible, due to the high load impedance and absence of any non-linearity. Immediately after 0.3 seconds, the load current is seen to increase rapidly. The waveforms after 0.3 seconds are identical to that in Fig. 4.3 (c).

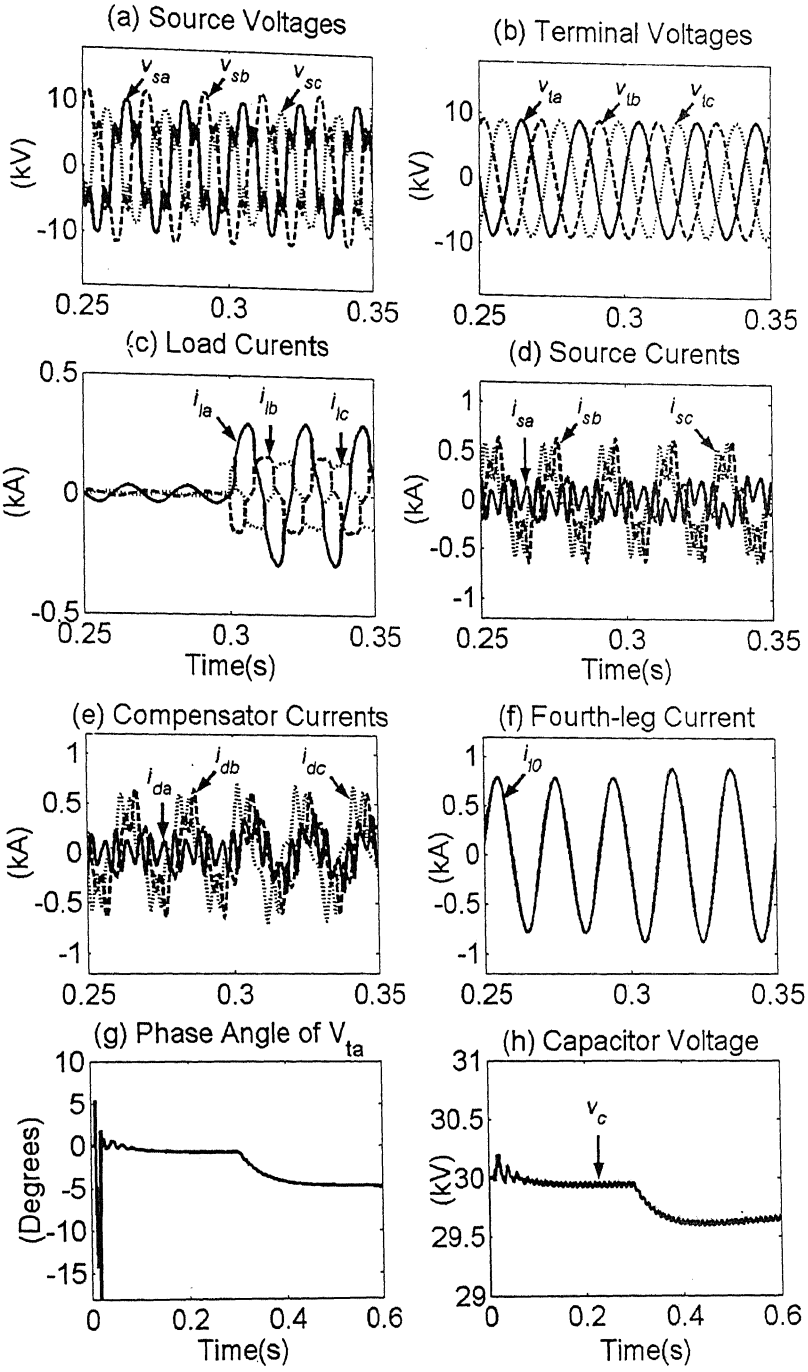

Fig. 4.4 System response with a DSTATCOM in the case of sudden increase in load current

Fig. 4.4 (g) shows the reference phase angle for the phase a of the PCC voltages. After initial oscillations, the phase angle settles to approximately -1° for the light load condition. After the load increases, more oscillations are observed and the phase angle settles to approximately –4.5°. Fig. 4.4 (h) shows the voltage of the DC storage capacitor. During light load condition, the voltage stabilizes to the reference value of 30 kV after oscillations. The load increase causes a dip in the voltage as the.

capacitor is supplying part of the increase real power demand of the load. Due to the action of the PI controller, the voltage begins to return back to 30kV. After time 2.05 seconds, the DC capacitor voltage settles at the reference value.

4.4 OPERATION OF THE DSTATCOM IN THE CASE OF VOLTAGE SAG

In this section, the behavior of the DSTATCOM as a voltage restorer is studied as opposed to its operation as a voltage regulator in the previous sections. Initially, the system parameters are considered to be the same as given in Table 4.1. After 0.3 seconds the source voltages are reduced to 70% of their initial values for a period of 0.2 seconds (10 cycles) after which the source voltages return to their initial values. The compensator must maintain the terminal voltages to be balanced sinusoids with a peak of 9 kV.

Fig. 4.5 shows the simulation results. Fig. 4.5 (a) shows the source voltages to be unbalanced and distorted and also shows the voltage sag occurring at 0.3 seconds. Fig. 4.5 (b) shows the terminal or the PCC voltages at the time the sag occurs. As can be seen, the voltage waveforms remain balanced sinusoids and are regulated at 9 kV peak. Fig. 4.5 (c) shows the PCC voltages at the time the sag is removed. The terminal voltages continue to be balanced sinusoids having a peak of 9 kV throughout the sag. Fig. 4.5 (g) shows the reference phase angle of the phase a terminal voltage. During the sag, the angle oscillates and settles to approximately -9°. The parameters of the PI controller have been set by trial and error to ensure that despite any voltage sag, the oscillations do not cause instability in the system. For larger values of K_p than the one chosen the system becomes unstable. After the sag is removed the phase angle settles at approximately –4.5° as in the simulations before. Fig. 4.5 (h) shows the voltage of the DC storage capacitor. During the voltage sag, the voltage dips with the corresponding fluctuations in the reference phase angle of the terminal voltage. After the sag is removed, the voltage begins to return back to its reference value of 30 kV. After time 1.5 seconds, the DC capacitor voltage settles to the reference value. The load currents are not shown here as the load is identical to the previous simulations.

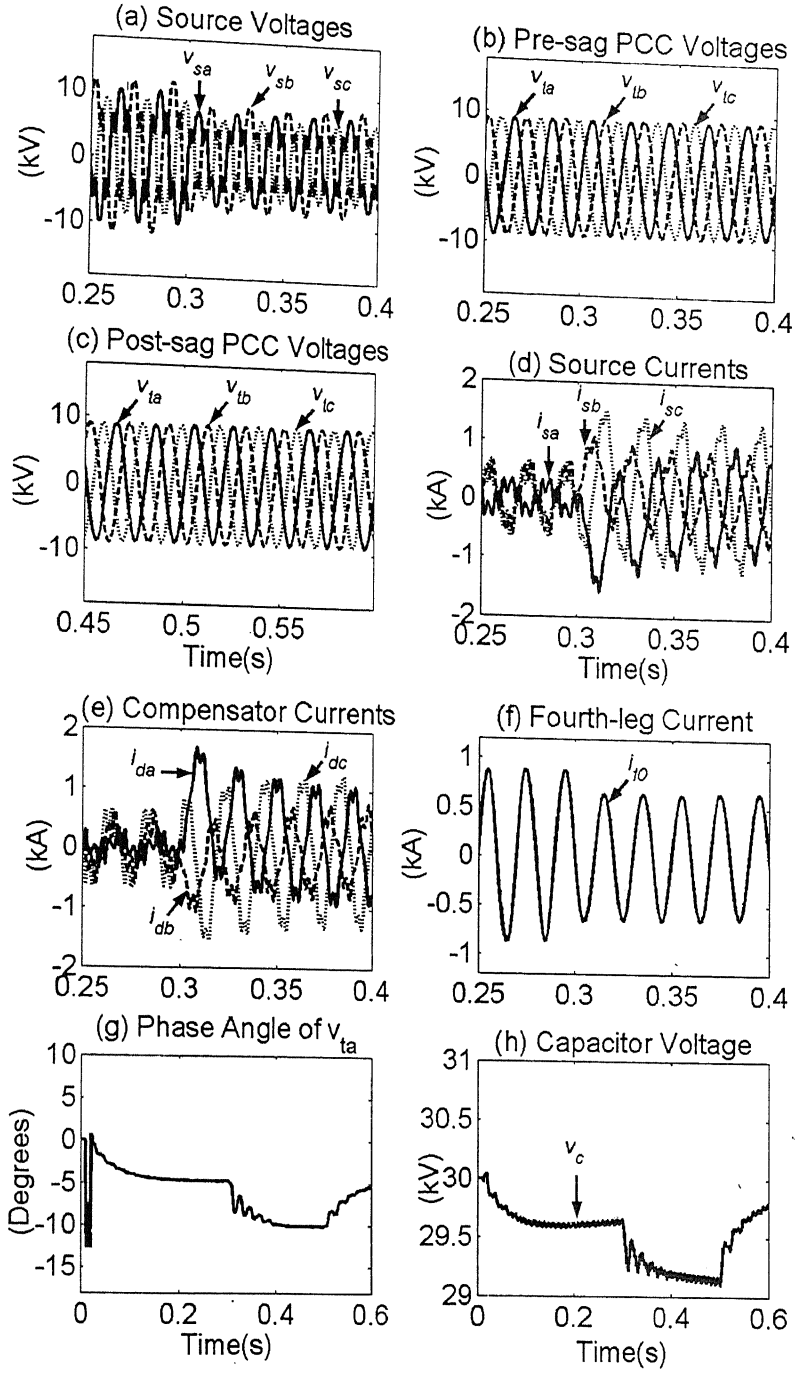

Fig. 4.5 System response with a DSTATCOM in the case of a 30% sag in source voltages

4.3 OPERATION OF THE DSTATCOM IN THE CASE OF VOLTAGE SWELL

The DSTATCOM has been shown to act as a voltage restorer and a voltage regulator in the case of a voltage sag in the previous section. A similar behavior can be

demonstrated in the case of a voltage swell. The system parameters are the same as in Table 4.1 and used in simulations before. The source voltages are initially at the same values considered in Table 4.1. After 0.3 seconds, a 30% swell in the source voltages occurs for a period of 0.2 seconds (10 cycles). The source voltages then return to their original values before the swell. The parameters of the PI controller and the feedback matrix are the same as in previous simulations.

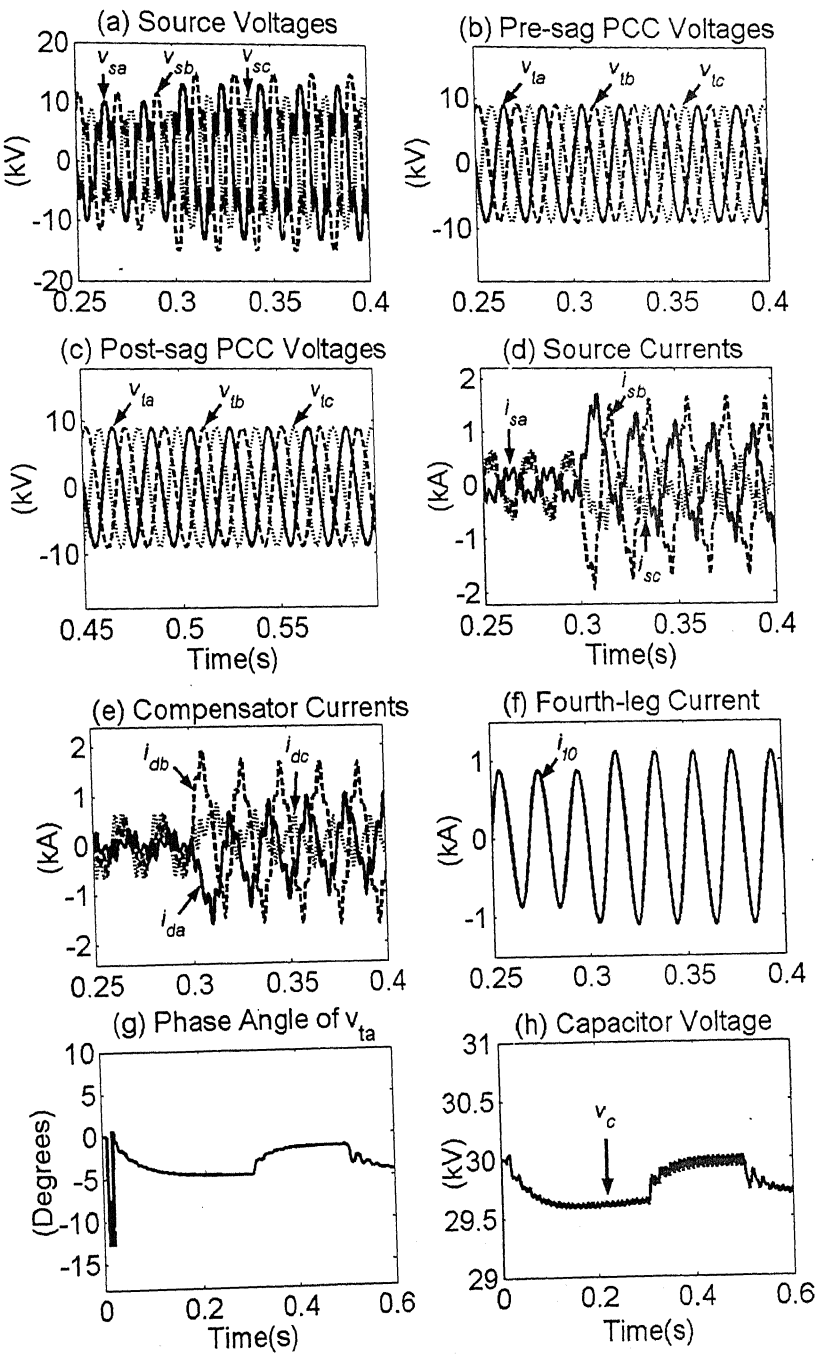

Fig. 4.6 System response with a DSTATCOM in the case of a 30% swell in source voltages

Fig 4.6 shows the simulation results. Fig. 4.6 (a) shows the source voltages before and during the swell. Fig. 4.6 (b) and (c) show the terminal voltages before and after the swell. The terminal voltages are balanced sinusoids and regulated at 9 kV peak during the transients when the swell occurs and the swell is removed. Fig. 4.6 (g) shows the reference phase angle of the phase a PCC voltage. When the swell occurs the phase angle oscillates and settles to approximately -2°. When the swell is removed the phase angle oscillates but finally settles to its steady state value of –4.5°. Fig. 4.6 (h) shows the voltage of the DC storage capacitor. The voltage fluctuates during the transients but begins to return back to the reference value of 30 kV. After time 2.1 seconds, the DC capacitor voltage settles at the reference value. In this case as well as the previous case, oscillations are observed during the transients but the terminal voltages are found to remain balanced sinusoids. Hence the parameters of the PI controller have resulted in stable operation of the compensator during normal operation as well as in the abnormal conditions without the system ever tending towards instability.

4.4 CONCLUSIONS

In his chapter, the DSTATCOM operating in the voltage control mode has been demonstrated for distortions and unbalance both in the source voltage as well as the load currents. Simulations have demonstrated stable operation of the DSTATCOM during changes in the load current as well as sag and sell in the source voltages with the load voltages being balanced sinusoids having a peak of 9 kV. The PI controller which regulates the DC capacitor voltage by controlling the phase angle of the load voltages, has been able to prevent the DC capacitor voltage from falling below 29 kV or rising above 31 kV during all disturbances. Hence the DSTATCOM in the voltage control mode has been shown to effective in regulating the load voltage despite disturbances in the source and load. However, the DSTATCOM has been seen to be injecting a very large magnitude of current into the system. The source currents are also seen to have large magnitude. The compensator and source currents increase even further when there is a sag or swell in the source voltages as shown in Fig. 4.5 and Fig. 4.6. Hence, the current rating of the compensator will have to very large and also the current rating of the feeder will have to be increased. As this could be inconvenient, the DSTATCOM in voltage control mode cannot be used widely to cover all the disturbances in the source side.

CHAPTER 5

DYNAMIC VOLTAGE RESTORER

In a distribution system the presence of non-linear loads causes the PCC voltages to become unbalanced and distorted. In the previous chapter, the DSTATCOM operating in the voltage control mode behaved as a voltage regulator and a voltage restorer thereby making the PCC voltages balanced sinusoids having a fixed peak. The disadvantage of this mode of operation is that since the DSTATCOM is a shunt compensator and is basically a current injection device, the current rating of the VSI would be very high. Moreover, if the source is stiff or the feeder impedance is negligible, voltage regulation of the PCC by current injection would become impossible. Hence, the present chapter discusses the Dynamic Voltage Restorer (DVR) that is a series compensation device as opposed to the DSTATCOM which is shunt connected. The chapter begins with the theory of series compensation. Two filter structures have been discussed and a comparison is drawn between them. For all simulations, the four-legged VSI with single DC storage capacitor discussed in Section 2.3.3 will be used.

5.1 THEORY OF SERIES COMPENSATION

Fig. 5.1 shows the single line diagram of a system with a DVR installed to protect a sensitive load [9]. The DVR has been modeled as an ideal voltage source injecting a voltage v_d. The capacitor C_f is a filter capacitor for filtering out the high frequency harmonics of the non-linear load.

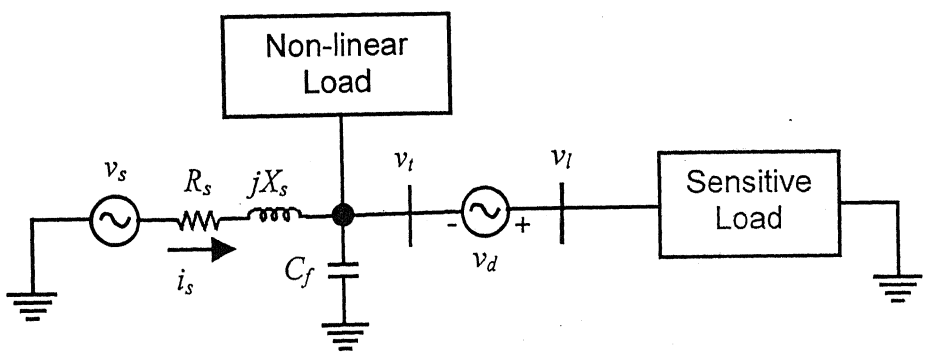

Fig. 5.1 Single-line diagram of a system with a DVR

From Fig. 5.1, the following expression can be written

$$v_l = v_t + v_d$$

Hence the reference for the injected voltage can be written as

$$v_d^* = v_l^* - v_t \tag{5.1}$$

As the DVR is required to maintain the voltage at the sensitive load at say an RMS value of V_{lm}, the reference phasor for the phase a load voltage can be written as

$$V_{la}^* = V_{lm} \angle \phi_{vla}^* \tag{5.2}$$

The phase angle ϕ_{vla} will determine the power absorbed or supplied by the DVR in the steady state. This is discussed in the next section.

5.2 RECTIFIER SUPPORTED DVR

Fig. 5.2 shows the single-line diagram of a DVR supported by a rectifier [19, 23]. In this circuit, the voltage of the DC storage capacitor is maintained by power fed through the uncontrolled rectifier from the source.

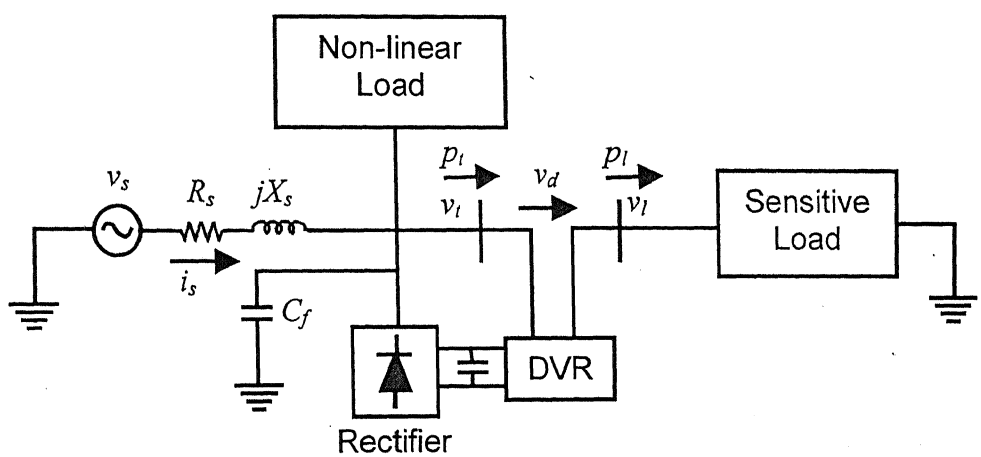

Fig. 5.2 Rectifier supported DVR

In the above case, the simplest method of setting the phase angle for the reference load voltage would be with respect to the phase angle of the fundamental positive sequence of the terminal voltage which can be determined by online Fourier extraction as given below

$$V_{ta1f} = \frac{\sqrt{2}}{T} \int_T \left(v_{ta} + \alpha v_{tb} + \alpha^2 v_{tc}\right) e^{-j(\omega t - \pi/2)} dt = \left|V_{ta1f}\right| \angle \phi_{ta1f} \tag{5.3}$$

where $\alpha = e^{j2\pi/3}$. Hence the phase angle for the reference load voltage for phase a can be set as follows

$$\phi^{*}_{vla} = \phi_{tal\,f} \pm \theta \tag{5.4}$$

where θ is an arbitrary small angle greater than zero. If the positive sign is taken, the load voltage will be leading in phase to the fundamental of the terminal voltage. Hence, the real power entering the terminal or the PCC bus will be greater than the real power entering the load bus. The excess real power will be absorbed by the DVR and will flow into the DC link. This reverse power flow may damage the diode rectifier. Hence, the reference load voltage is made to lag the fundamental of the terminal voltage by a small angle. This will ensure that the diode rectifier will always supply an average real power to the DC link and the DVR will always supply an average real power to the system. The phase angle for the references for the phases b and c will lag the phase angle for the reference for phase a by 120° and 240° respectively.

Two filter structures for the DVR will be considered. One of the structures uses a capacitor filter while the other uses an LC filter. In this section, control strategies for both the structures will be discussed and a comparison will be drawn between them.

5.3 DVR SUPPORTED BY A DC BATTERY

The control strategies for the two filter structures mentioned above will be developed for DVR supported by DC battery. These control strategies will then be applied to the rectifier supported DVR.

5.3.1 DVR with Capacitor Filter

The single-phase equivalent circuit for the DVR using the capacitor filter [9, 20] in Fig. 2.9 is shown in Fig. 5.3. All parameters of the compensator are referred to the secondary of the transformer. In this equivalent circuit the source is considered to be non-stiff with L_s and R_s as the inductance and resistance of the feeder. L_{Ts} and R_{Ts} are the leakage inductance and winding resistance of the transformer referred to the secondary. The load is modeled as an arbitrary RL load.

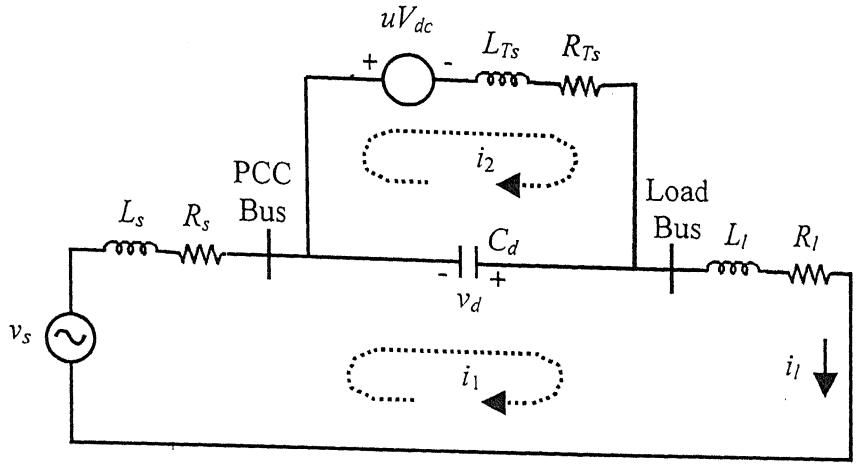

Fig. 5.3 Single-phase equivalent circuit of a DVR with a capacitor filter in the secondary of isolation transformer

Before discussing the rectifier supported DVR the control strategy will be developed by considering a DC battery as the energy source as shown in Fig. 5.3. To derive the state space equations for the above structure the state vector is chosen as

$$\boldsymbol{x} = \begin{bmatrix} i_1 \\ i_2 \\ v_d \end{bmatrix}$$

Hence, the state space equation can be written as

$$\dot{\boldsymbol{x}} = \begin{bmatrix} -\dfrac{R_s + R_l}{L_s + L_l} & 0 & \dfrac{1}{L_s + L_l} \\ 0 & -\dfrac{R_{Ts}}{L_{Ts}} & -\dfrac{1}{L_{Ts}} \\ -\dfrac{1}{C_d} & \dfrac{1}{C_d} & 0 \end{bmatrix} \boldsymbol{x} + \begin{bmatrix} 0 \\ -\dfrac{V_{dc}}{L_{Ts}} \\ 0 \end{bmatrix} u_c + \begin{bmatrix} \dfrac{1}{L_s + L_l} \\ 0 \\ 0 \end{bmatrix} v_s \qquad (5.5)$$

$$\dot{\boldsymbol{x}} = \mathbf{A}\boldsymbol{x} + \mathbf{B}_u u_c + \mathbf{B}_w v_s \qquad (5.6)$$

The output variable is the voltage across the filter capacitor

$$y = v_d = [0 \quad 0 \quad 1]\boldsymbol{x} \qquad (5.7)$$

$$y = \mathbf{C}\boldsymbol{x} \qquad (5.8)$$

For controlling the switching of the VSI a full state feedback control is used [9, 10]. The reference for the injected capacitor voltage can be obtained by the procedure discussed before in this section and can be given by Eqn (5.1). To use state feedback

control a reference for the current i_2 is required which can be obtained by applyin KCL at the PCC bus as follows

$$i_2^* = i_l + C_d \frac{dv_d^*}{dt} \tag{5.9}$$

By choosing a feedback matrix $\boldsymbol{K}$, the control input can be determined a follows

$$u_c = -\boldsymbol{K}(\boldsymbol{x} - \boldsymbol{x}_{ref}) \tag{5.10}$$

This control input can be further subjected to hysteresis control to generate th switching control logic as follows

If $u_c > h$ $u = 1$

$u_c < -h$ $u = -1$

Where h is the hysteresis band.

The reference for the current to be tracked by the fourth leg of the inverter wi be the zero sequence component of the references for the injected currents. If th primary to secondary turns ratio of the transformer is k then the reference for the fourt leg current is given by

$$i_0^* = k(i_{2a}^* + i_{2b}^* + i_{2c}^*)$$

This reference current is tracked using simple hysteresis current control.

Simulation results:

Table 5.1 shows the system parameters considered for the simulation. Th reference for the load voltage has been set to lag the fundamental positive sequence the terminal voltage by an angle of 5° and has a peak of 9 kV. A Linear Quadrat Control (LQR) is employed to determine the feedback matrix $\boldsymbol{K}$. The following state weighting matrix $\boldsymbol{Q}$ and control weighting r are chosen

$$\boldsymbol{Q} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 20 & 0 \\ 0 & 0 & 100 \end{bmatrix}, \quad r = 1.0$$

Table 5.1 System Parameters

System Parameters	Values of Parameters
Source voltages	$V_{an} = 6.35\angle 0°$ kV $V_{bn} = 7.35\angle -140°$ kV $V_{cn} = 5.35\angle 110°$ kV
Feeder Impedance	$R_s + jX_s = 0.5 + j3.141\ \Omega$
Non-Linear Load at PCC	Diode Rectifier having the following load $R + jX = 350 + j12.56\ \Omega$ Filter capacitor $C_f = 50\ \mu$F
Sensitive load	Balanced load of $R_l + jX_l = 75 + j31.41\ \Omega$
Compensator Parameters	$V_{dc} = 3$ kV $C_d = 50\ \mu$F $L_{d0} = 4$ mH, $R_{d0} = 0.01\ \Omega$. 3.3kV/22kV, 5 MVA transformer with leakage reactance of 10% and $R_{Ts} = 0.01\ \Omega$

The feedback matrix is obtained by using the Control Systems Toolbox in MATLAB and is found to be

$$\boldsymbol{K}' = [0.1838 \quad -0.1905 \quad -0.3684]$$

With the above feedback matrix, the eigenvalues of the closed loop system are to the left of the straight line s = -1990.9. The first term of the $\boldsymbol{K}'$ matrix corresponds to the load current as can be observed from Eqn. (5.10). As the load is likely to change frequently, a reference for the load current is difficult to set. Hence, the feedback matrix is reduced to

$$\boldsymbol{K} = [0 \quad -0.1905 \quad -0.3684]$$

This causes a change in the eigenvalues of the closed loop system which are now to the left of the straight line s = -1980.6. This minimal shift in the eigenvalues will not affect the stability of the closed loop system.

Fig. 5.4 shows the simulation results. Fig. 5.4 (a) shows the PCC or the terminal voltages to be both unbalanced and distorted. Fig. 5.4 (b) shows the voltages at the sensitive load that are balanced sinusoids and regulated to a peak of 9 kV. Fig. 5.4 (c) shows the sensitive load currents. These are balanced and sinusoidal as the sensitive load is balanced. Fig. 5.4 (d) shows the average real powers in the system. The average load real power is greater than the average real power entering the PCC or the terminal

bus. Hence the DVR is supplying a very small amount of average real power to the load and the curve of the average real compensator power is very close to zero. The switching frequency of the VSI is approximately 4.5 kHz.

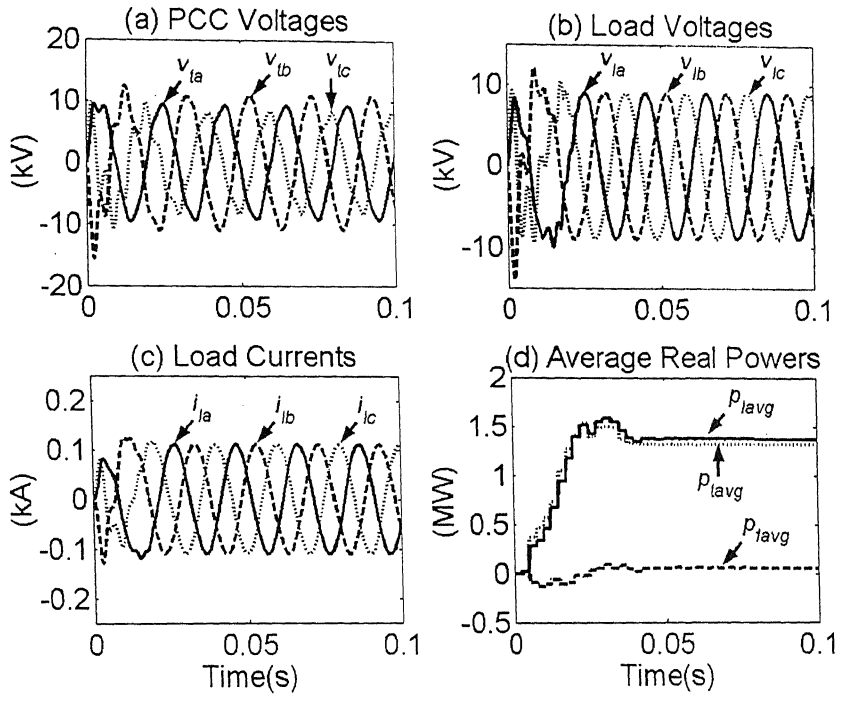

Fig. 5.4 System responses with a DVR using capacitor filter and supported by a DC battery.

5.3.2 DVR with LC Filter

The complete circuit diagram of the DVR with LC filter [9, 20, 21] is shown in Fig. 5.5. Fig. 5.6 shows the single-phase equivalent circuit of the DVR with the LC filter. All parameters of the source, feeder and load are referred to the primary of the transformer.

In the circuit below L_d and C_d form the LC filter while L_{Tp} and R_{Tp} are the leakage inductance and winding resistance of the transformer referred to the primary. From the above figure it is evident that the voltage injected by the DVR is not the same as the voltage across the filter capacitor C_d. The reference for the injected voltage is given by Eqn (5.1) as

$$v_{inj}^{*} = v_{l}^{*} - v_{t} \tag{5.11}$$

As the winding resistance of the transformer referred to the primary is negligible, the reference for the filter capacitor voltage can be written in terms of the reference for the injected voltage as follows

$$v_d^* = v_{inj}^* + L_{lp}\frac{di_1}{dt} \tag{5.12}$$

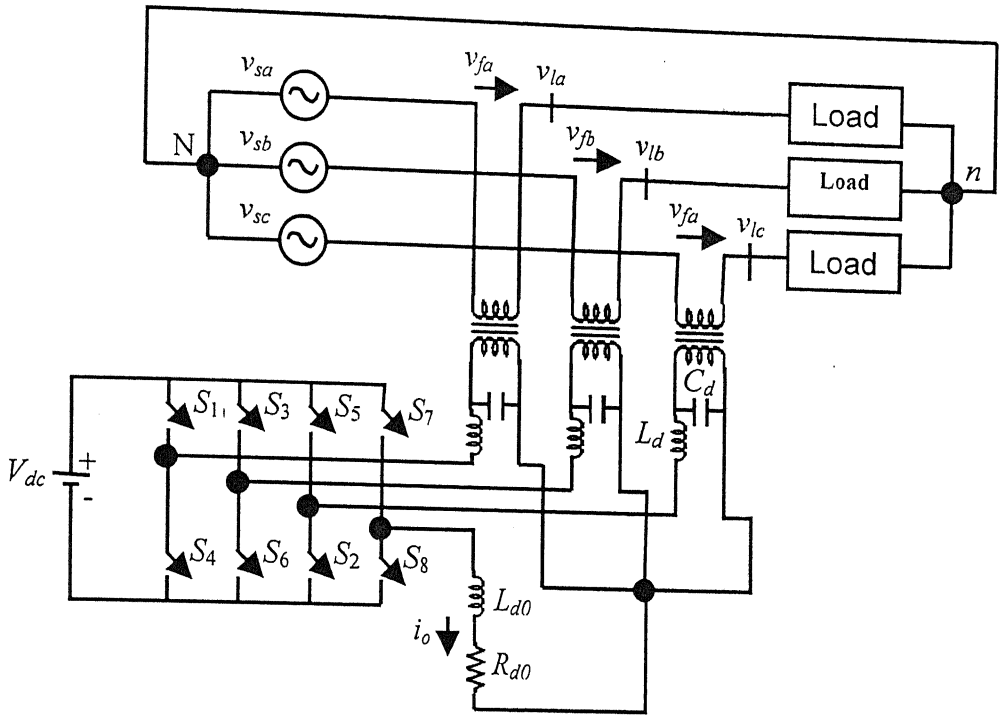

Fig. 5.5 DVR using four-leg VSI with LC filter in the primary of isolation transformer

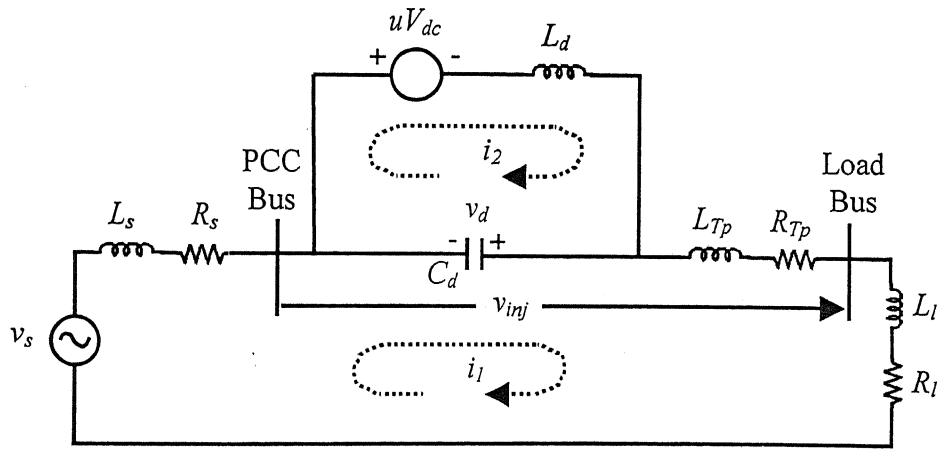

Fig. 5.6 Single-phase equivalent circuit of a system with a DVR using an LC filter in the primary of the isolation transformer

As before, the state vector is chosen to be

$$x = \begin{bmatrix} i_1 \\ i_2 \\ v_d \end{bmatrix}$$

Hence, the state space equation can be written as

$$\dot{x} = \begin{bmatrix} -\frac{R_s + R_T + R_l}{L_s + L_{Tp} + L_l} & 0 & \frac{1}{L_s + L_{Tp} + L_l} \\ 0 & 0 & -\frac{1}{L_f} \\ -\frac{1}{C_d} & \frac{1}{C_d} & 0 \end{bmatrix} x + \begin{bmatrix} 0 \\ -\frac{V_{dc}}{L_{Tp}} \\ 0 \end{bmatrix} u_c + \begin{bmatrix} \frac{1}{L_s + L_{Tp} + L_l} \\ 0 \\ 0 \end{bmatrix} v_s \qquad (5.13)$$

$$\dot{x} = \mathbf{A}x + \mathbf{B}_u u_c + \mathbf{B}_w v_s \qquad (5.14)$$

The output variable is the voltage across the filter capacitor

$$y = v_d = [0 \quad 0 \quad 1]x \qquad (5.15)$$

$$y = \mathbf{C}x \qquad (5.16)$$

The reference for the current i_2 can be obtained in a manner similar to the previous section given by Eqn. (5.9). The reference current for the fourth leg is given by

$$i_0^* = i_{2a}^* + i_{2b}^* + i_{2c}^*$$

The reference current for the fourth leg is tracked by simple hysteresis current control

By choosing a suitable feedback matrix the control input u_c can be obtained from Eqn. (5.10) and the switching control input u will be obtained by subjecting u_c to hysteresis control as in the previous section.

Simulation Results :

Considering the system parameters given in Table 5.1 and identical to that in section 5.2.1, the simulation is repeated. The compensator parameters are as follows

$$V_{dc} = 3 \text{ kV}$$

$$C_d = 600 \text{ μF}, L_d = 1 \text{ mH}$$

To determine the feedback matrix an LQR is employed and the following weighting matrices are chosen

$$\boldsymbol{Q} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 75 \end{bmatrix}, \qquad r = 1.0$$

The feedback matrix is obtained using the Control Systems Toolbox in MATLAB. The feedback matrix is found to be

$$\boldsymbol{K}' = [0.0312 \quad -0.0355 \quad -0.2686]$$

The eigenvalues of the closed system are found to be left of the line s = -1957. To avoid the need to generate references for the load current, the feedback matrix is reduced to

$$\boldsymbol{K} = [0 \quad -0.0355 \quad -0.2686]$$

The eigenvalues of the closed system are found to be left of the line s = -1954. This minimal shift in the eigenvalues of the closed loop system will not affect the stability of the system.

Fig. 5.7 shows the simulation results. These simulation results can be seen to be very similar to the results shown in Fig. 5.4 for the DVR with capacitor filter. The switching frequency if found to be approximately 4.2 kHz.

Though the performance of the DVR with the capacitor filter and the LC filter are very similar there will be a difference in the power loss in the two cases when practical implementation is attempted. In the DVR with the capacitor filter, the filter is connected across the secondary of the transformer which removes switching frequency harmonics from the injected voltage. However the primary of the transformer is still subjected to the switching frequency harmonics generated by the VSI. Hence the losses in the transformers will be higher. In the case of the DVR with the LC filter, the filter is connected in the primary of the transformer. Hence the transformer is not subjected to the switching frequency harmonics generated by the VSI. Hence the DVR with the LC filter is chosen for further simulations involving the rectifier supported DVR.

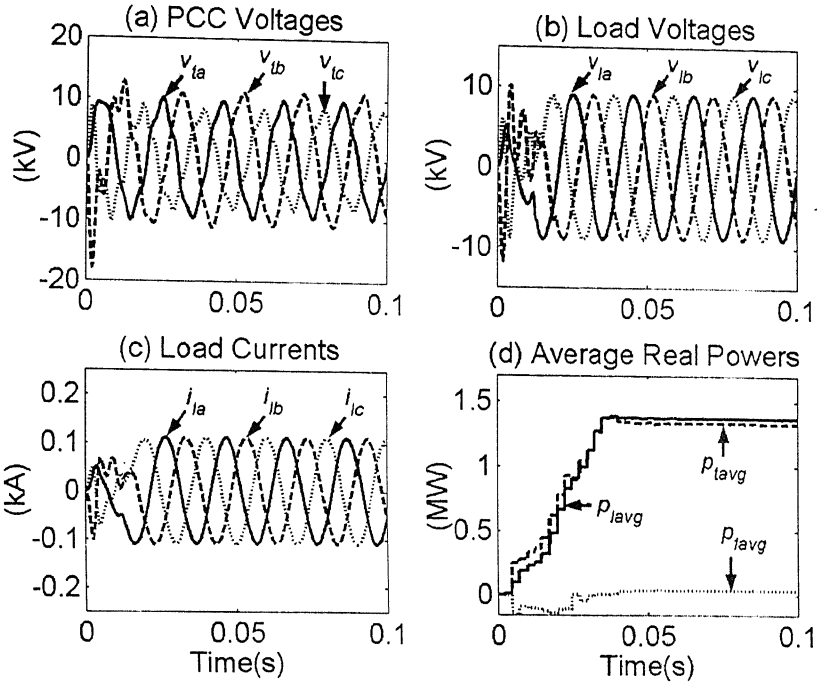

Fig. 5.7 System response with a DVR using an LC filter and supported by a DC battery

5.4 SIMULATION OF RECTIFIER SUPPORTED DVR

Before presenting the simulation results, the auxiliary power supply to the DC storage capacitor shall be examined closely. Fig. 5.8 shows the single-line diagram of the circuit feeding the DC storage capacitor C_{dc}.

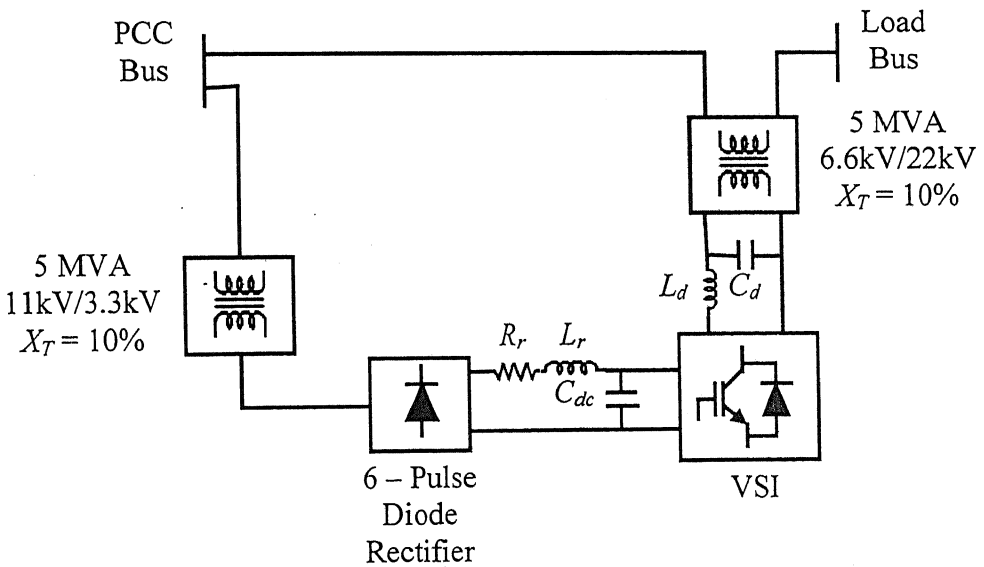

Fig. 5.8 Single-phase circuit showing the diode-rectifier, VSI and LC filter

For the circuit above the values for R_r and L_r are 1.0 Ω and 1.0 mH respectively. The DC storage capacitor has a value of 10000 μF. All other parameters of the system including the filter parameters of the series compensator are identical to the simulation with the DC battery as the energy source for the DVR. The feedback matrix is given by

$$K' = [0.01 \quad -0.0178 \quad -0.1343]$$

The eigenvalues of the closed system are found to be left of the line s = -12203. To avoid the need to generate references for the load current, the feedback matrix is reduced to

$$K = [0 \quad -0.0178 \quad -0.1343]$$

The eigenvalues of the closed system are found to be left of the line s = -12139. This minimal shift in the eigenvalues of the closed loop system will not affect the stability of the system.

Fig. 5.9 shows the simulation results. The waveforms in Fig. 5.9 (a)-(d) are similar to the waveforms from the previous simulations. As before the DVR is supplying a small amount of average real power to the system. Hence, the average real power demand of the load is greater than the average real power entering the PCC. Fig. 5.9 (e) shows the voltage of the DC storage capacitor that is charged through the diode rectifier and the voltage is seen to settle at a value of approximately 4.8 kV. It is to be noted that the primary terminals of the transformers in the VSI of the DVR have a voltage rating of 6.6 kV. The reason for choosing a 6.6kV/22kV transformer is to prevent saturation in the transformers. If a 3.3kV/22kV transformer is to be used as in the previous simulations but saturation in the transformers is to be prevented, the voltage of the DC capacitor must be prevented from exceeding 3.3 kV. In order to achieve this, a controlled rectifier is used in place of an uncontrolled rectifier as described in the next section.

5.5 DVR SUPPORTED BY A CONTROLLED RECTIFIER

In the single-line diagram of Fig. 5.8 the 6-pulse diode rectifier is replaced with a 6-pulse thyristor-based full converter. The isolation transformers in the VSI are 3.3kV/22kV transformers instead of 6.6kV/22kV transformers. All other parameters

remain the same. The firing angle of the thyristors in the full converter are set according to the voltage of the DC storage capacitor.

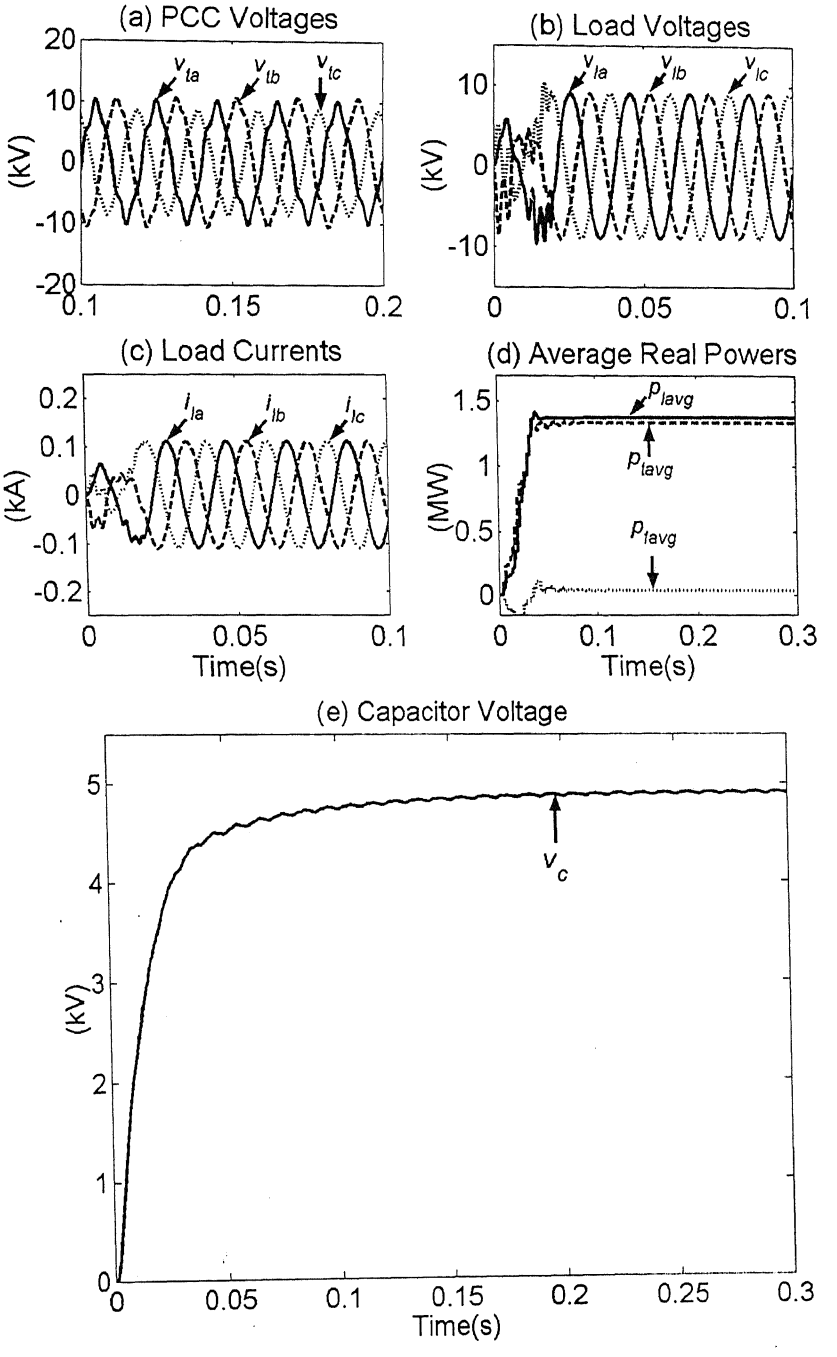

Fig. 5.9 System response with a DVR supported by an uncontrolled rectifier

If the capacitor voltage is less than 3 kV, then the firing angle is set to zero and hence the converter will behave in a similar manner to the diode rectifier. When the capacitor voltage exceeds 3 kV, the firing angle is set to 170°. In this case, the DC capacitor supplies power back to the PCC.

The feedback matrix is the same as in the simulation of Section 5.3.2. Fig. 5.10 shows the simulation results. The waveforms shown in Fig. 5.10 (a)-(d) are once again similar to the waveforms obtained in previous simulations. Fig. 5.10 (e) shows the voltage of the DC storage capacitor. The capacitor voltage is not allowed to rise well above 3 kV because the change in the firing angle of the thyristors causes it to fall back. Hence saturation of the transformers of the VSI is prevented.

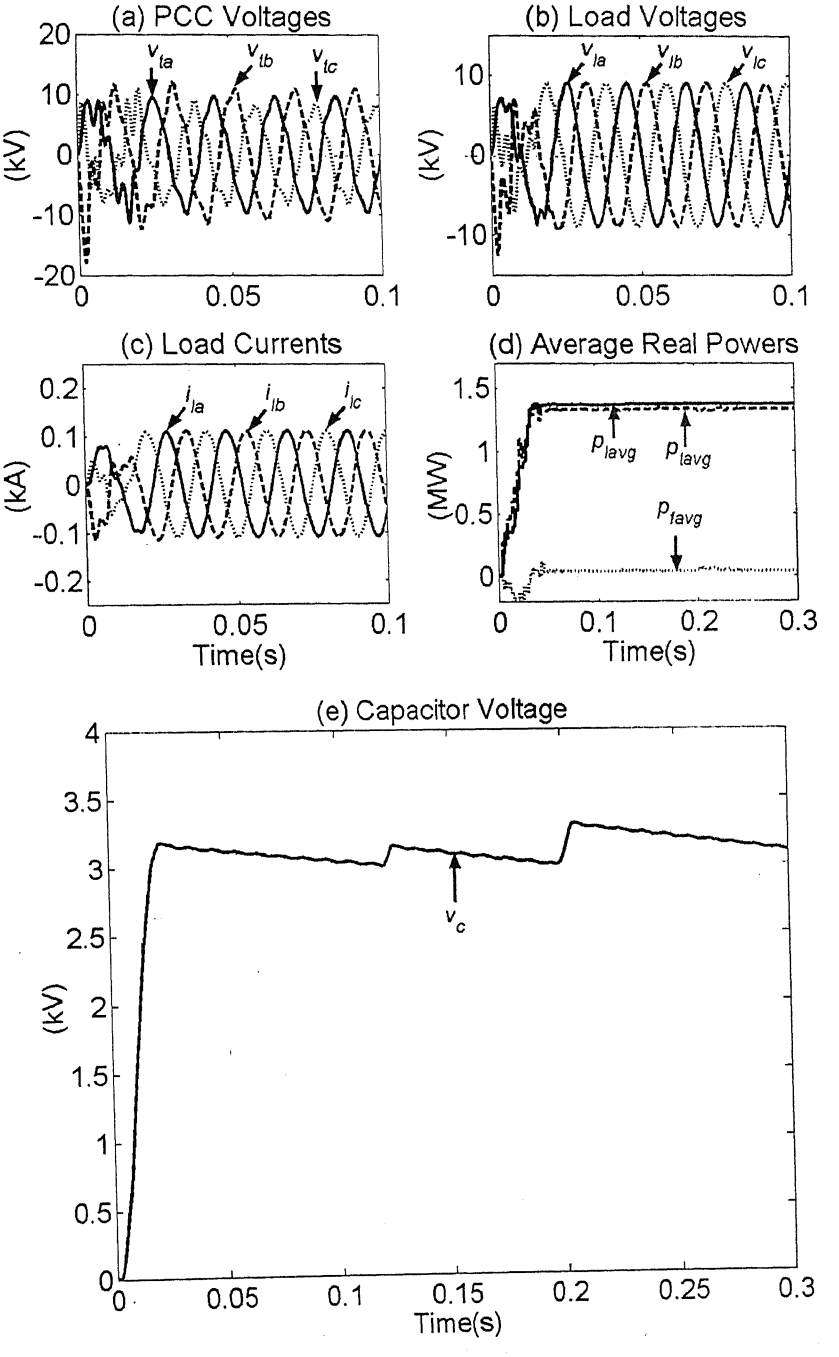

Fig. 5.10 System response with a DVR supported by a controlled rectifier

5.6 OPERATION OF THE DVR IN THE CASE OF VOLTAGE SAG

In all previous simulations the source voltages were considered to have a constant magnitude throughout the simulation. The operation of the DVR shall now be examined in the case when there is a sag in the source voltages [22, 23, 24]. The DVR should maintain the load voltages to be balanced sinusoids and at a peak of 9 kV throughout the sag.

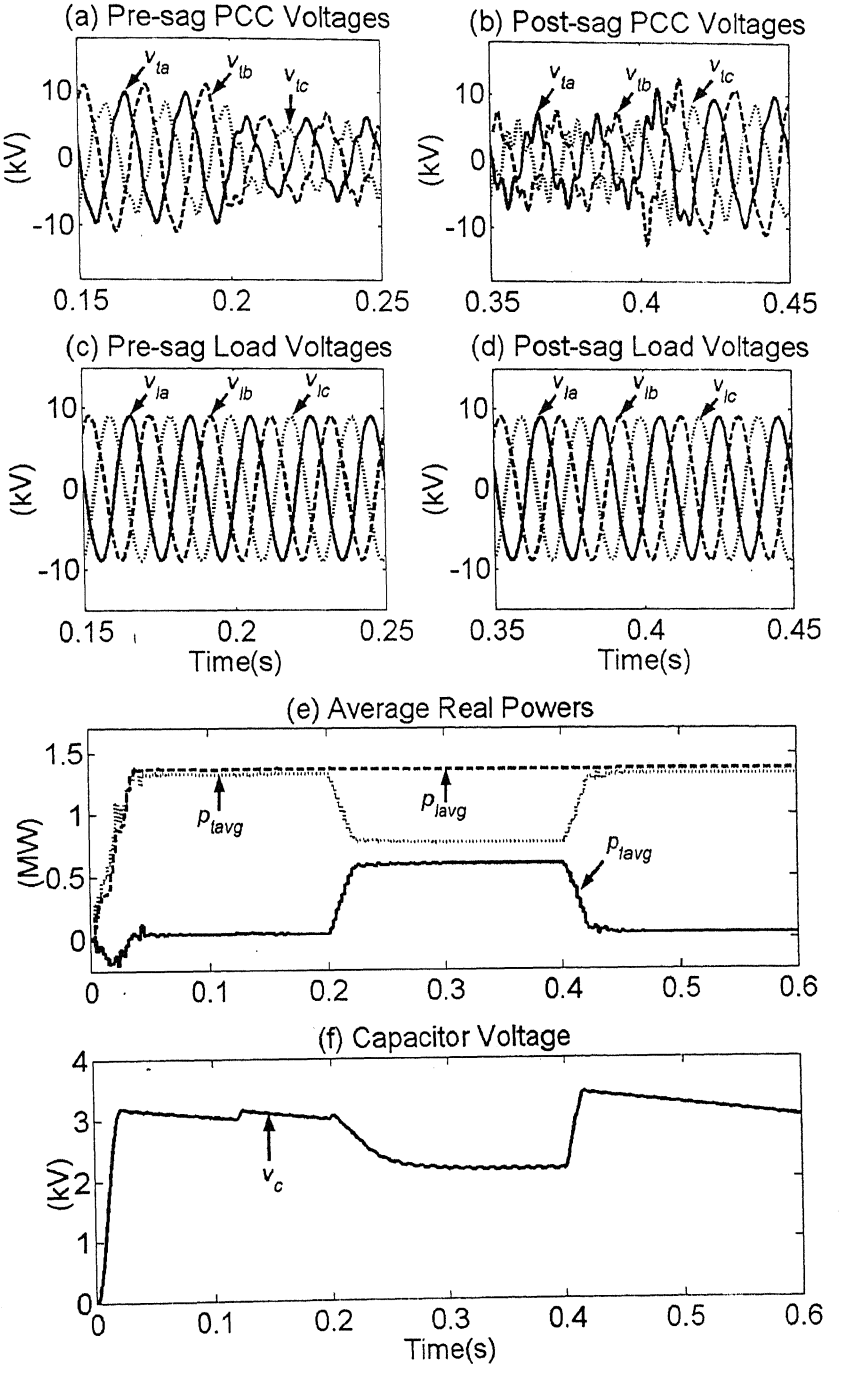

Fig. 5.11 System response with a DVR during 40% voltage sag

The source voltages are initially at the values specified in Table 5.1. After 0.2 seconds a 40% sag is produced in the source voltages for a period of 0.2 seconds (10 cycles). The source voltages are restored to their original values after 0.4 seconds. All other system parameters are the same as in the simulation before. Fig 5.11 shows the simulation results. Fig. 5.11 (a) and (b) show the PCC voltages when the sag occurs and the sag is removed respectively. Fig 5.11 (c) and (d) show the load voltages during the same time periods as the PCC voltages. The load voltages remain balanced sinusoids and at 9 kV peak despite the transient in the PCC voltages. Fig. 5.11 (e) shows the average real powers. During the sag the DVR supplies a large amount of real power to the load. Fig. 5.11 (f) shows the DC storage capacitor voltage which drops during the sag and recovers when the sag is removed. During the sag the capacitor voltage settles to a new lower value rather than to fall continuously as it draws real power from the PCC through the converter. Hence the DVR has been able to protect the sensitive load completely during the sag.

5.7 CONCLUSIONS

In this chapter, a DVR topology has been proposed as a compensation device to protect a sensitive load from all disturbances from the source side or from non-linear loads connected to the PCC. The simulation results show the load voltages to be smooth balanced sinusoids regulated to a peak of 9 kV. The DVR supplies a small amount of average real power to the system in the steady state which is supplied to the DC link by a controlled rectifier. This auxiliary source of power to the DC link enables the DVR to provide complete protection to the sensitive load during a deep voltage sag as has been shown in the last simulation. Hence the performance of the DVR as a device for load voltage regulation for both normal as well as adverse circumstances has been proved.

CHAPTER 6

CONCLUSION

The general conclusions from the thesis and the scope for future work have been presented in this chapter.

6.1 GENERAL CONCLUSIONS

The general conclusions from the thesis can be summarized as follows

1. A comparison of the VSI topologies used for the DSTATCOM and the DVR has been presented. The comparison has been supported by simulation results and for both the DSTATCOM and the DVR the four-leg VSI with single DC capacitor has been selected as being the most suitable.
2. The theory of active and reactive power in three-phase four-wire networks has been discussed and an algorithm has been derived for shunt compensation in systems with unbalanced and distorted source voltages. Different control strategies such as hysteresis current-control, pole shift control and LQR control have been used to control the switching of the VSI in the DSTATCOM. The method to maintain the DC capacitor voltage despite rapid changes in the load by drawing or supplying real power from the system has been studied. Simulation results have been provided to show that the DSTATCOM has been able to provide full compensation in systems with unbalanced and non-linear load drawing a DC component when the source voltages are balanced sinusoids as well as when they are unbalanced and distorted.
3. The DSTATCOM in the voltage control mode has been studied and simulated. The simulations have covered several types of disturbances in the load and source and the PCC voltages have been shown to be balanced sinusoids with a fixed peak. Moreover, the DC capacitor voltage has been shown to not deviate considerably from the reference value and returns back to the reference value after a certain period of time (1 to 2 seconds).
4. The theory of series compensation has been studied. Two different filter structures along with the control strategies for controlling the switching of the VSI have been studied. The DC capacitor has been provided with an auxiliary source of power

through a rectifier and the DVR has been simulated in the case of a deep sag in the source voltages.

6.2 SCOPE FOR FUTURE WORK

Based on the research already done in the field of shunt and series compensation and the work presented in this thesis, the scope for future work can be summarized as follows

1. A review has been performed for control strategies for switching the VSI. Other forms of current controllers such as adaptive hysteresis controller, constant frequency based hysteresis controller and space vector modulation can be implemented and compared. Other control algorithms such as sliding mode control and Linear Quadratic Gaussian (LQG) can be implemented.
2. Instead of using DC capacitors as the energy source of the inverters, other forms of renewable energy such as fuel cells can be used. In the DVR, a rectifier supported the DC capacitor so that the DVR could compensate for deep sags over a prolonged period of time. Instead the DC capacitor voltage could be regulated at the reference value by drawing real power for the system and be supported by a fuel cell during deep sags or complete outage of the source.
3. Instead of using the DSTATCOM and DVR alone with their separate energy sources, they could be used together with a common DC capacitor to form a Unified Power Quality Conditioner (UPQC). The UPQC could maintain the source currents to be balanced sinusoids and regulate the load bus voltages to be balanced sinusoids having a fixed peak despite the load currents and source voltages being unbalanced and distorted.

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